Cost-Effective Use of HDI (microvia) PCB Technology for SI, PI and EMC

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High Density Interconnect (HDI) PCB manufacturing technology

- Also known as microvia technology, or Sequential Build-Up technology (or simply ‘Build-Up’)...
  - uses ‘microvias’ 6 thou (0.15mm) diameter or less, so can achieve twice the number of pins/area than THP...
  - and which only connect between necessary board layers, so don’t constrain routing on other layers
- All of which means they can significantly reduce the number of PCB layers required...
  - especially where THP would require 10 layers or more

Features of original HDI technology

- Traditional drilled via
- ‘Buried’ microvias
- A drilled via on the inner FR4 core only
- FR4 core
- ‘Blind’ microvias
- Pure polymer build-up layers

Modern HDI can ‘stack’ vias


Microvias are closed at one end...

- so don’t steal solder during reflowing, allowing via-in-pad layouts...
  - good for EMC because this reduces the inductances associated with power supply decoupling
- But if blind microvias-in-pads are not completely filled/capped to provide a planar copper surface...
  - solder paste printed over them traps little air bubbles...
  - which expand and ‘pop’ during soldering, possibly causing poor solder joints

HDI benefits

- HDI techniques help to make the smallest, lightest, and least power-hungry products...
  - and can be found in a wide variety of common products (including some toys)
- Microvias are inherently more robust than THP...
  - so are preferred in some hi-reliability or harsh environment applications
Typical ‘dog-bones’ under a BGA
from http://diag-laptop.pl/

Copper filled/capped via-in-pad means no pin-escapes or ‘dog bones’
(can use THP or HDI)

Via-in-pad microvias do not have to be on a regular grid (matrix) – can be moved around to ease routing on layers below

December 2011: 6.8 billion transistors
4 stacked silicon dies, 19 Watts at 180,000 MIPs

Exploded view of Xilinx Vertex-7

Microvias with via-in-pad in the chip’s substrate (connect metal bumps on the silicon to BGA for PCB)

BGA’s PI & SI suffers from perforation of the 0V, Power planes underneath

■ The best that can be done with THP is to use suitable track-and-space (track-and-gap) layout rules…
  – to try achieve a complete mesh or grid over the area covered by the BGA’s solder pads…
    ■ as discussed in my previous Webinar, on June 25, 2014
Example of poor plane meshing under BGAs
from: ‘Figure 18-8, CAM Artwork Screen Shots, Example #1, 144-ball csBGA’,
Lattice Semiconductor Technical Note TN1074: ‘PCB Layout Recommendations
for BGA Packages’, Sept. 2013

Example of good plane meshing under BGAs
from: ‘Figure 18-10, CAM Artwork Screen Shots, Example #1, 256-Ball
csBGA’, in Lattice Semiconductor Technical Note TN1074: ‘PCB Layout
Recommendations for BGA Packages’, Sept. 2013

HDI 0V planes aren’t perforated…
– and so create solid, continuous 0V/Power plane pairs
under BGAs, with lower series inductances, higher
mutual inductances and higher capacitances which all
improves decoupling…
  • improving both PI and EMC
– and they provide lower and more constant return path
  inductances…
  • improving both SI and EMC

Where microvias do perforate a plane, the gaps
they create are very small…
– so the effects on SI, PI and EMC are small

HDI’s additional EMC benefits include…
– via-in-pad reduces decoupling inductances, pushing
  PDN resonances to higher frequencies…
– shorter traces become efficient ‘accidental antennas’
  at higher frequencies…
– smaller PCBs become efficient “accidental patch
  antennas” at higher frequencies…
– shorter traces may not need to be treated as
  transmission lines…
– less perforated 0V and Power planes have improved
  ‘image plane’ effect so have higher shielding
effectiveness

HDI makes it possible to use the
smallest IC package styles, and
obtain their EMC benefits, e.g…
– Miniature or Micro BGA (especially with ball pitch <1mm)
– DCA (direct chip attach)
– Flip-chip
– CSP (chip scale packaging)
– TAB (tape automated bonding)

These very small, thin semiconductor packages
have much closer proximity to the PVB’s 0V/Power
planes than a regular packaged IC…
– so their ‘image plane’ effect is stronger –
  reducing emissions, and increasing immunity

Poll Questions
Beware, when using chip-scale package styles!

- Because they lack the inductances associated with bond wires and lead-frames...
  - their very sharp internal switching speeds ‘leak’ higher levels of higher frequency noises into the PCB structure, making EMC worse...
  - unless HDI and good EMC design techniques are used

HDI suppliers and technologies

- In May 2000 there were 62 manufacturers of HDI boards worldwide, and in May 2008 there were 32 manufacturers just in the UK...
  - their manufacturing techniques can vary, and may need different layout techniques, so always check with chosen manufacturer before starting board layout
- Basic standard: IPC-2315 (from www.ipc.org)...
  - some good EMC PCB design techniques were made impractical by original HDI technology...
  - e.g. 0V/Power plane pairs adjacent to top/bottom sides...
  - made practical again by modern microvia technologies

HDI costs

- An IPC survey in 2000 found HDI boards could be purchased for the same cost as THP...
  - and not using buried vias helps reduce costs further
- Latest advice (Mentor Graphics) is that boards needing > 8-10 layers should cost less if made in HDI...
  - e.g. a high-density 18 layer THP board would only need 10 layers if using HDI...
  - but even for lower densities or fewer layers, HDI’s EMC, SI and PI advantages make it more cost-effective than THP...
  - focussing on the BOM cost instead of ‘overall cost of manufacture’ is a common management mistake!

Some modern microvia technologies

(These ones are from Viasystems, visit: www.viasystems.com/technology/hdi.html)

1) Stacked or Second Generation MicroVias (SMV®)
2) Deep Microvias (DpMV™)
3) Deep Stacked MicroVias (DpSMV™)

These types claimed to provide a planar surface for via-in-pad BGAs, and have improved current capacity & thermal management

More examples of modern microvia techniques

IPC Type I construction: ‘IPC Type I’ from “HDI Layer Stackups for Large Dense PCBs”, by Happy Holden and Charles Pfeil, Mentor Graphics, July 2007

- IPC Type I has microvias & THP vias, and laminated core (e.g. FR4) with a single microvia layer (e.g. pure polymer) on at least one side
- Note: no buried THP vias
**IPC Type II**

Basic IPC Type II

- At least one microvia layer (e.g. pure polymer) on each side of the core (e.g. FR4)
- THP vias are drilled in the laminated core, become buried when the microvia layers are added
- Micro-vias may be stacked or are staggered relative to buried vias on other layers
- THP vias may also be drilled and plated through the whole layer stack

**IPC Type II with variable-depth microvias**

(e.g. Skip microvias)

**IPC Type II with stacked microvias**

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**IPC Type III**

Basic IPC Type III

- At least two micro-via layers on at least one side of the core
- THP vias are drilled in the laminated core, become buried when the microvia layers are added
- Micro-vias may be staggered or stacked with themselves and/or with buried THP vias
- The whole layer stack may have THP vias

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**Some HDI stack-up issues**

- IPC Types I, II and II use a core (e.g. FR4) with FR4 or polymer ‘build-up’ layers containing microvias and/or THP vias, to keep costs low...
  - but different layer materials have different temperature coefficients and rates of moisture absorbance...
    - so delamination is a real possibility, especially if there is significant temperature and/or humidity cycling...
    - not a problem, of course, when using same material for every layer
- Some people say: “IPC Type IV, V, VI HDI constructions are more costly, and probably not necessary for large dense PCBs with BGA breakout and routing challenges”

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**Stack-ups for good PI and EMC**

From: “HDI Layer Stackups for Large Dense PCBs”, by Happy Holden and Charles Pfeil, Mentor Graphics, July 2007

- Top and Bottom layers as 0V (i.e. GND) planes helps shield all the internal traces...
  - with perimeter guard traces and low-cost BLS (board level shields) can make fully-shielded PCB assemblies...
    - see my PCB book for more details...
  - usually 30% or more BGA pins are 0V and many of the rest are Power, but microvia antipads are very small...
    - so the perforation of these planes is not very great
- Power (VCC, VDD) planes on adjacent layers create distributed (embedded) decoupling capacitances immediately below the devices: best for PI
Stack-ups for good PI and EMC continued...

- These stackups benefit from stacked microvias, and board size, product weight/size, and overall manufacturing costs can be reduced by:
  - embedded pull-up and termination resistors...
  - embedded surge/transient protection...
  - embedded ICs (like smart cards)...
  - embedded decoupling capacitors...
  - embedded high-capacitance laminates

  Ideally less than 50µm (0.002 inch) thick, between 0V/Power planes, can provide several nF per square centimetre, making it possible to eliminate all soldered decoupling capacitors (excluding ‘bulk’ caps ≥ 10µF)

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Some useful sources for HDI (microvia)


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Poll Questions

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Some useful sources for HDI (microvia) continued...

- IPC-2315, “Design Guide for High Density Interconnects & Microvias”, and a number of other standards and guides on HDI, Build-up, and Microvia PCB technology, including IPC-2226, IPC-4104, IPC-6016 and IPC-9151, can be purchased on-line from IPC at www.ipc.org

_Chip Clough Consulting Ltd_
Some useful sources for HDI (microvia) continued...


Some useful sources for HDI (microvia) continued...


- "Power Integrity Effects of High Density Interconnect (HDI)", by Happy Holden, available from Mentor Graphics® index at www.mentor.com/techpapers/fulliment (search for HDI) or direct from: www.mentor.com/pcb/resources/overview/power-integrity-effects-of-high-density-interconnect-hdi-a4c6125f-12b7-44ad-9d51-1323c4a8552 (many other good HDI papers from this Mentor Graphics® index: search by ‘HDI’)


Some useful sources for embedded/buried PCB components continued...


- "Reduce PCB Impedance, Noise, and EMI and Simplify PCB Layout!", describes 3M™ Embedded Capacitance Material (ECM), http://solutions.3m.co.uk/wps/portal/3M/en_GB/EmbeddedCapacitanceMaterial/Home/


Other useful sources

  not available via Amazon or other distributors, who might indicate that it is out of print when in fact it is printed on demand. This 2nd Edition is identical to the 1st Edition except for size/format – if you have the 1st Edition, no need to buy the 2nd!