

Design Techniques for EMC

Part 0 — Introduction

and

Part 1 — Circuit design and choice of components

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This is the first in a series of six articles on basic good-practice electromagnetic compatibility (EMC) techniques in electronic design, to be published during 2006. It is intended for designers of electronic modules, products and equipment. To avoid having to write modules/products/equipment throughout – everything that is the result of a design process will be called a ‘product’.

This series is an update of the series first published in the UK EMC Journal in 1999 [1], and includes basic good EMC practices relevant for electronic, PCB and mechanical designers in all applications areas (household, commercial, entertainment, industrial, medical and healthcare, automotive, railway, marine, aerospace, military, etc.). Safety risks caused by electromagnetic interference (EMI) are not covered here, see [2] for more on this issue.

These articles deal with the practical issues of what EMC techniques should generally be used and how they should generally be applied. Why they are needed or why they work is not covered, but they are well understood academically and well proven over decades of practice. A good understanding of the basics of EMC is a great benefit in helping to prevent under- or over-engineering, but goes beyond the scope of these articles.

The techniques covered in these six articles will be:

- 1) **Circuit design (digital, analogue, switch-mode, communications), and choosing components**
- 2) Cables and connectors
- 3) Filters and transient suppressors
- 4) Shielding
- 5) PCB layout (including transmission lines)
- 6) ESD, surge, electromechanical devices, power factor correction, voltage fluctuations, supply dips and dropouts

Many textbooks and articles have been written about all of the above topics, so this magazine article format can do no more than introduce the various issues and point to the most important of the basic good-practice EMC design techniques. References are provided for further study and more in-depth EMC design techniques.

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0. Introduction to the series

0.1 Cost-effectiveness and time-to-market

Many designers still tend to focus on the functionality and performance of their designs, leaving most of the EMC issues until the last minute, when their product appears to be substantially complete and can be tested for EMC compliance. But almost the one thing that all EMC design experts agree on is that this approach is *guaranteed* not to be the most cost-effective, and also *almost guaranteed* to add avoidable delays to the project's overall timescale and the product's market introduction.

As electronic technologies advance, integrated circuits and transistors are generally becoming more vulnerable to electromagnetic (EM) phenomena, whilst the circuits they are used in become greater sources of unwanted electromagnetic noise (emissions). The electromagnetic spectrum is becoming more heavily utilised, whilst simultaneously becoming more 'polluted'. The overall result is that the financial penalties for not 'designing-in' EMC from the start of each new project are continually increasing.

Designing-in EMC always looks as if it is going to increase the cost of the bill of materials (the 'BOM cost') – but by the time a design is EMC compliant and ready for market it has usually decreased the BOM cost. Even where the final BOM cost is higher, the true cost of manufacture and the profitable selling price will usually be lower. (BOM cost is not in fact a major determinant of the profitable selling price for the vast majority of products, despite what generations of badly-informed managers might have said.)

The profitable 'sales life' of a new product is continually decreasing, with very few products lasting for more than 2 years before being significantly upgraded or lasting for more than 5 years before being replaced. The effect of this is that since 2000, time-to-market has generally been a more important factor than the cost of manufacture, in the lifetime return on investment of a new product.

This six-part series hopes to make designers aware of the basic EMC techniques that should *a/ways* be taken into account during any new design. As time progresses and technology advances, these techniques become more and more necessary and need to be implemented in more depth and with greater attention to detail.

For more on these issues see Part 1 of [3].

0.2 The project EMC lifecycle

Before starting on the EMC design topics in this series, it is useful see them in the context of the ideal EMC lifecycle of a design and development project, as follows...

- Establishment of the target EM specifications for the new product, including:
 - The EM environment it must withstand, including continuous, high-probability, and low-probability disturbances, see [4].
 - The permissible degradation in performance to be allowed during disturbance events.
 - Its possible proximity to sensitive apparatus and allowable consequences, hence its emissions specifications.
 - Whether there are any safety issues requiring additional EM performance specifications. Safety compliance in the event of EMI is covered by safety directives and standards, not by the EMC Directive and its standards, see [2].
 - All the EMC standards to be met, regulatory compliance documentation to be created, and how much “due diligence” to apply in each case (consider all markets, any customers’ in-house specifications, etc.).
- System design:
 - At least employ basic system-level EMC good-practices, such as those described in [5] and [6]. More advanced techniques may be necessary for compliance or cost-effectiveness.
 - Flow the ‘top-level’ EMC specifications down into the various system blocks.
- System block (electronic) designs:
 - At least employ the basic good-practices in EMC design covered by these six articles. More advanced techniques may be necessary for compliance or cost-effectiveness.
 - Experiment, calculate or simulate the EMC of designs prior to creating any hardware, perform simple EMC tests on early prototypes [7], perform more standardised EMC tests [7], [8] on later prototypes and/or first production versions.
- Employ basic good-practice EMC techniques in software design, see [9] and Chapter 37 of [10].
- Achieve regulatory compliance for all target markets.
- Employ EMC testing and other techniques in QA to control:
 - Product consistency due to tolerances and changes in components (e.g. IC die-shrinks) and variations in assembly and other manufacturing processes.
 - Changes in assembly, including wiring routes and component substitutions.
 - Design modifications (electrical, electronic, mechanical, software) including software bug-fixes.
 - All variants and upgrades.
- Sell only into the markets originally designed for;
 - To add new markets go through the initial electromagnetic specification stage again.
- Investigate all complaints of interference problems
 - Feed any resulting improvements to design back into existing designs and new products (a corrective action loop).

This may look quite daunting, but it is only what successful professional marketeers and engineers already know to do, so as not to expose their company to excessive commercial, financial or legal risks.

1. Circuit design and choice of components for EMC

Correct choice of active and passive components, and good circuit design techniques used from the beginning of a new design and development project, will help achieve EMC compliance in the most cost-effective way, reducing the cost, size, and weight of the eventual filtering and shielding required.

These techniques also improve digital signal integrity and analogue signal-to-noise, and can save at least one iteration of hardware and software. This will help new products achieve their functional performance specifications, and get to market, earlier. These EMC techniques should be seen as a part of a company’s competitive edge, for maximum commercial benefit.

EMC standards are being developed for testing the emissions and immunity of active devices, so in the future we can look forward to being able to compare device EMC specifications directly.

1.1 Digital: choosing active devices and circuit design

1.1.1 Choosing active devices

Most digital devices operate with pulse trains, which have a very large harmonic content. Figure 1A shows how the harmonic content of two example square waves is affected by the frequency and by the rise/fall time of the digital edges. The higher the frequency, and the sharper the edges, the worse the emissions will generally be. So always choose the lowest clock rate and slowest rise/fall times that will still achieve the functional specification. For example, do not use 74AC when 74HC will do, and do not use 74HC when CMOS 4000 would be adequate.

The rise/fall time specifications are almost always maximum values, to allow the manufacturers to use smaller silicon processes to save cost without having to modify their data sheets. So the actual rise/fall times of the integrated circuits (IC) on a printed circuit board (PCB) can be very much less than their specification suggests, generally between one-quarter and one-tenth depending on the silicon process used. As time goes on, devices are generally made with smaller silicon processes, so their real-life rise/fall times decrease and emissions increase.

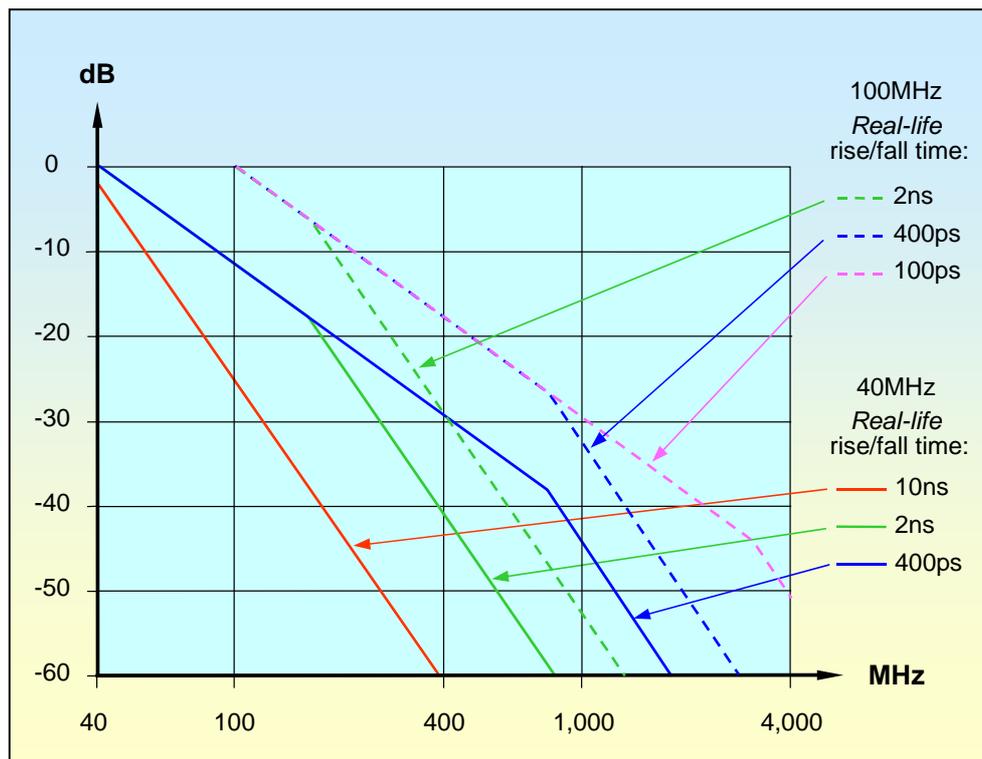


Figure 1A The effect of rise and fall time on the envelope of a squarewave's harmonics

Devices with specified EMC features or performance are preferred (preferably with minimum and maximum specifications, where appropriate), including...

- *Adjacent, multiple, or centre-pinned power and ground.* (The old TTL pinout standard that placed power and ground pins at the opposite corners of an IC creates the maximum EMC and ground-bounce problems.)
- *Reduced output voltage swing and controlled slew rates.* These reduce the dV/dt and dI/dt and so reduce emissions. Reduced output swing could possibly worsen immunity in some situations, so a compromise may be needed.
- *Reduced emissions.* Most manufacturers offer glue-logic ranges with reduced emissions, for instance ACQ and ACTQ have lower emissions than AC and ACT. Some offer VLSI in "EMC friendly" versions, for example Philips have at least two 80C51 microprocessor models which are up to 40dB quieter than other 80C51s, and Fujitsu Mikroelektronik offers the F²MC-16LX family of microprocessors. Some FPGA and ASIC designers can also offer devices with reduced emissions.

Some FPGAs and ASICs allow slew rate, output drive capability and/or impedance of their output signals to be controlled. They can help save time in development stages.

- *Increased immunity.* Many types of serial communications devices (RS232, RS 485, USB, etc.) are available with increased immunity to electrostatic discharge (ESD) on their I/O pins. If their immunity

performance isn't specified to at least the same standards and levels that you need for your product, additional suppression components will be needed.

- *Low input capacitance devices.* These help to reduce the current peaks that occur whenever a logic state changes, and hence reduce the magnetic fields and ground return currents (both prime causes of digital emissions). In transmission-line applications they help match the line.
- *On-chip (or in-package) decoupling capacitance.* This is the best location for decoupling for EMC, and also makes PCB power rail decoupling much easier.
- *On-chip (or in-package) memory.* So that no high-data-rate buses are required on their printed circuit boards.
- *Reduced levels of power supply transients.* When 'totem-pole' circuits in ICs change state, they pass through a brief period when both upper and lower devices are on at the same time, momentarily shorting the supply rail. The resulting power supply current transient (sometimes called 'shoot-through') can exceed the signal's current. Shoot-through noise causes emissions from the power supply distribution network.
- *Drive current rating no greater than required.* Drivers rated for a higher output current have larger output transistors, which generally means increased power supply transient currents and 'shoot-through' noise emissions.
- *Low ground-bounce.* Such devices will generally be better for EMC. When outputs switch simultaneously, their ground bounces add up to create much larger noise voltages. ASIC and FPGA designers have certain tricks they can use to prevent simultaneous switching, such as placing different numbers of buffers in the output-enables of the output drivers. See page 20-16 of [10].
- *Plenty of 0V pins.* The best devices for EMC have *at least* as many 0V pins as all of the other pins put together, with the 0V pins spread all through the other pins.
- *Non-saturating logic.* For devices with the same maximum operating frequency, non-saturating logic devices (e.g. ECL) have lower rise/fall times and much lower power supply transient currents (shoot-through) compared with saturating logic types such as TTL, so have significantly lower emissions.
- *High-speed devices with internal clock generators.* These generally cause lower emissions than devices which use external clock generators. Some devices have internal clock-multipliers, phase-locked-loops that lock onto a low rate system clock, and this is better for emissions than distributing a high-speed system clock.
- *Differential ('balanced') signalling.* These devices use \pm differential signals and do not use the 0V as their signal return. They help reduce emissions and improved immunity when driving high-speed signals.
- *Transmission-line matching I/Os.* ICs with outputs capable of matching to transmission-lines are needed when high-speed signals have to be sent down long conductors. E.g. bus drivers are available which will drive a 25Ω shunt-terminated load. These will drive a single 25Ω transmission line (e.g. RAMBUS); or two 50Ω lines; four 100Ω lines or six 150Ω lines (e.g. using star-connection).
- *Prefer devices that have EMC application information.* Suppliers of some ICs provide detailed EMC design application notes (as Intel does for its Pentium MMO ICs). So always ask whether detailed EMC data exists, get a copy and follow it closely.

But always check that the guidance follows modern good EMC practices – such as those described in this series. For example, many device application notes still repeat the out-dated advice to split 0V planes between analogue and digital PCB areas. This and many other techniques cannot control RF above a few MHz, so were good advice before the 1960s (when they were first developed) but are unhelpful in the modern world where all conductors can now be expected to suffer from significant levels of noise at up to 2.45GHz (getting higher in level and frequency all the time).

- *Asynchronous (naturally clocked) devices.* Asynchronous technology, also called 'clockless', 'handshake' and 'naturally clocked' has much lower emissions than synchronous logic, and also much lower power consumption. At least one asynchronous IC design tool is now commercially available. Philips has been developing asynchronous processors for many years, now spun off as a separate company called Handshake Solutions.

1.1.2 Designing digital circuits

- *Rise/fall time control.* To reduce emissions we want to use rise and fall times that are as slow and smooth as possible, especially for long PCB traces and wired interconnections. But many manufacturers don't specify their device's rise or fall times at all, or else only specify the maximum values (which does not help).

It is increasingly the case that digital devices switch much faster than is needed for functionality, so we often find ourselves having to suppress unwanted harmonics. For the greatest cost-effectiveness, this should be done right at the devices concerned – so it is a good idea to make provision on PCBs for control of logic edge speed or bandwidths, as shown by Figure 1B, at least on prototypes.

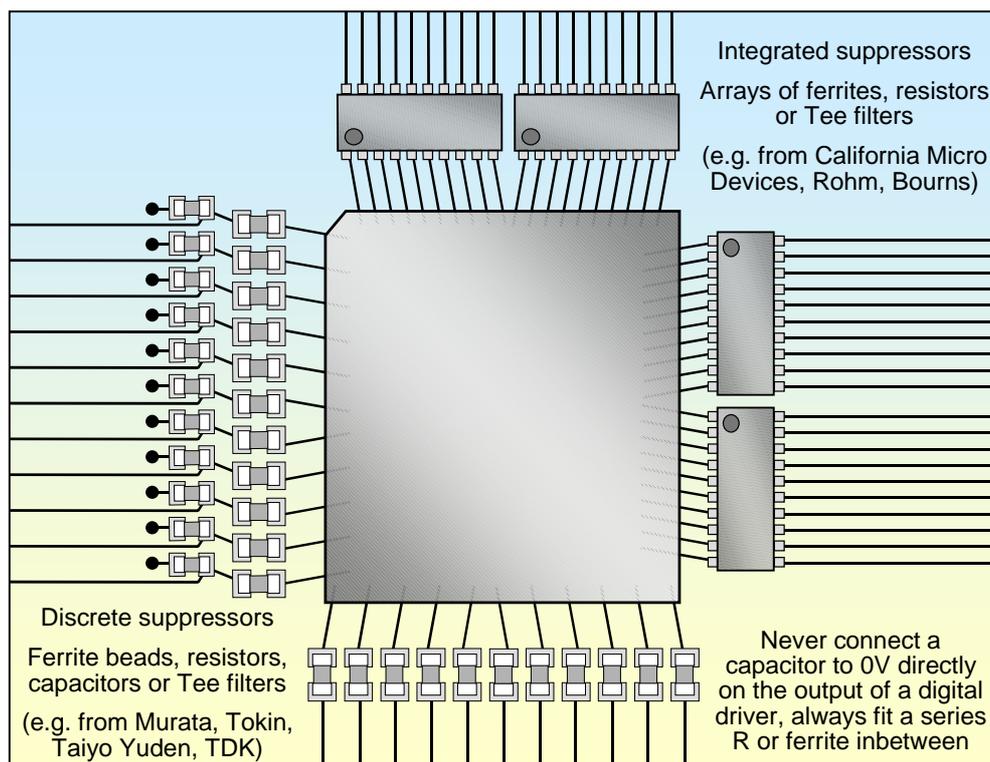


Figure 1B Making provision on the PCB for controlling unwanted harmonics

Series resistors or ferrite beads are usually the best way to control edge rates and unwanted harmonics, although R-C-R tee filters can also be used and may be able to give better control of harmonics where transmission lines are used. (simple capacitors to ground can increase output transient currents and increase emissions.) Where skew is not a problem very slow edges should be used, 'squared-up' with Schmitt gates at the receiving end if necessary.

On prototype PCBs the series suppression components can be shorted-out at first by zero-ohm components or traces that can easily be cut with a scalpel. Shunt components (capacitors) might not be fitted at first. If it becomes evident that an IC is causing emissions that are too high, at frequencies that are not required for circuit functionality, the suppression components can then be fitted.

- *Position any open-collector pull-ups near to their drivers, and use high values.* This reduces the maximum current in the trace and the area of its current loop, so helps to reduce emissions. But it could worsen immunity performance in some situations, so a compromise may be needed.
- *Power supply decoupling.* This is needed at every power or reference voltage pin, and is discussed in the forthcoming Part 5 of this series, and in Part 5 of [1].
- *Connect all unused gates (inputs) to 0V or V+ rail (whichever is appropriate).* This is best done via a pull-down or pull-up resistor, to allow the gate to be exercised during testing or fault-finding, and to prevent high currents in programmable I/O pins when the program is 'buggy' or corrupted by EMI.
- *Noisy PCB traces.* PCB traces carrying clock signals, and similar signals that 'toggle' at high rate (e.g. R/W strobes, output enables and chip selects) are usually the worst offenders for emissions, and the placement of the relevant devices, trace layout and routing are very important, and covered in the forthcoming Part 5 of this series, Part 5 of [1], and in more detail in [3].
- *Clock buffering.* When a clock signal must travel a long distance to drive a number of loads, fit clock buffers near to groups of loads so the long trace (or wire) has smaller currents in it, to reduce its emissions.
- *Check for 'runt' pulses.* Some devices and some circuit techniques create runt pulses – also called 'glitches' – pulses that are not proper logic transitions. Apart from the problems they can create for signal integrity and reliable operation, they are a cause of increased emissions. So avoid devices and circuit techniques that cause runt pulses, and always spend some time checking the actual waveforms with a

high-speed oscilloscope and probes to ensure that runt pulses do not occur in practice. Page 21-9 of [10] has more on this.

- *Avoid bus contention.* When two devices try to take control of a bus at the same time, high levels of emissions can occur. See page 21-8 of [10] for more on this.
- *Do not mix clock and I/O buffers in the same package.* The crosstalk between the buffers in the package will 'pollute' the I/O lines with clock noise, increasing emissions.
- *Do not mix on-board and off-board signal buffers in the same package.* The crosstalk between the buffers in the package will 'pollute' the off-board signals with on-board noise, increasing emissions.
- *Microprocessor watchdog design.* Interference often occurs in bursts lasting for hundreds of milliseconds, or even seconds. A watchdog which is supposed to restart a processor will be no good if it allows its processor to be crashed or hung permanently by later parts of the same burst that first triggered the watchdog. So the watchdog should be designed around an astable oscillator that keeps on 'barking' until the processor is fully operational once more.

As soon as the watchdog has restarted the microprocessor, it should start timing-out again and reset/restart the micro again if it has not received a 'tick' from the micro to indicate the software is running properly again. An edge-triggered watchdog is also a good idea, so that the watchdog function is not defeated by a 'stuck bit' and cannot hold the micro's reset pin in restart mode continuously. The watchdog must control the reset pin, not an interrupt even a non-maskable one. See 7.2.3 of [11] for more on watchdogs.

Programmable devices can have their programs corrupted by EMI, so should not be used for watchdogs.

- *Use a power supply monitor.* Power supply dips, dropouts, interruptions, sags, and brownouts can make the logic DC rail drop below the level required for the correct operation of microprocessors and similar devices. Simple resistor-capacitor 'power-on reset' circuits are not adequate – an accurate power monitor (sometimes called a 'brownout monitor' or 'brownout detector') is required to protect memory writes and prevent erroneous control activity.

Programmable devices can have their programs corrupted by EMI, so should not be used for power supply monitors.

- *Matched transmission line techniques.* These help reduce emissions and improve immunity when the rise/fall time of a digital signal is less than about eight times the propagation delay (t_p) along the full length of its conductor (whether a PCB trace, wire or cable). PCB transmission line design and matching is discussed briefly in the forthcoming Part 5 of this series, in Part 5 of [1], and in more detail in Part 6 of [3].

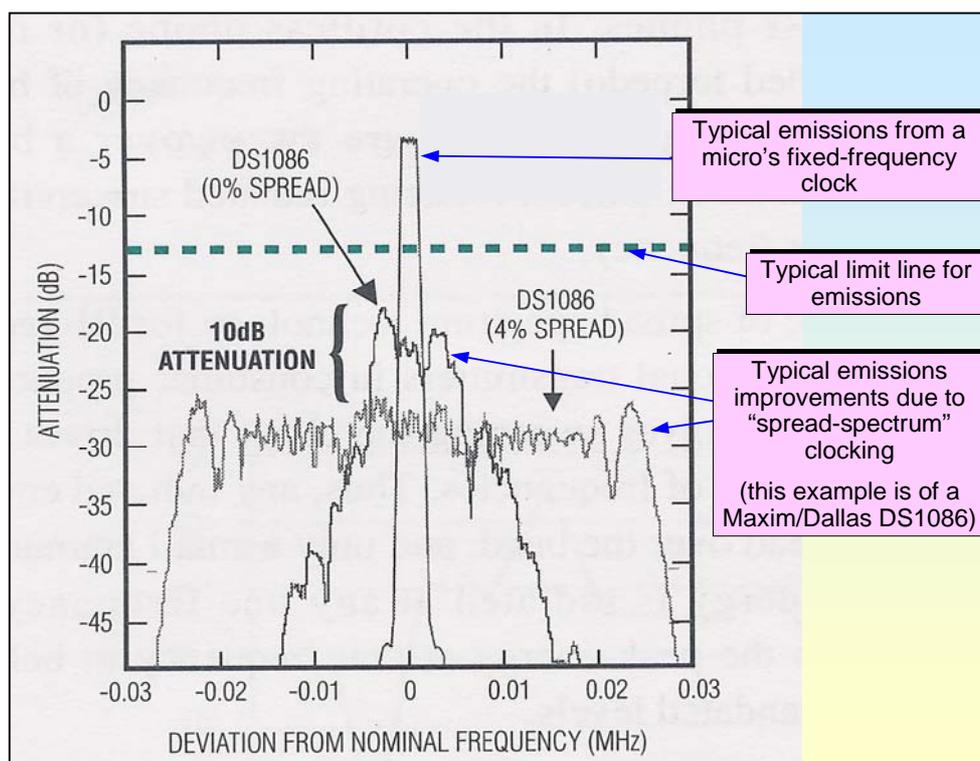


Figure 1C Example of spread-spectrum clocking

- *Spread-spectrum clocking.* Emissions from clocked digital devices, switch-mode power converters, and their circuits have a spectrum consisting of many very narrow lines at the fundamental frequency and its harmonics. Each line has a very narrow bandwidth. But the filters used by EMC receivers and spectrum analysers for conducted emissions testing are 9kHz wide, and for radiated emissions testing they are 120kHz wide (specified in CISPR 16-1), so the emissions appear to be either 9kHz or 120kHz wide even though they are in fact much narrower. CISPR 16-1 also specifies that the Quasi-Peak (QP) and Average (AV) detectors used for emissions measurements are integrators that have an averaging response.

Modulating the frequency of the digital or switch-mode clock moves the frequency of each emission line around rapidly, and if the range of movement exceeds the 9 or 120kHz bandwidths of the emissions measurements the result will be a lower QP or AV detector output at each line frequency. Figure 1C shows an example of the effects of replacing a standard crystal oscillator with a proprietary spread-spectrum clock oscillator.

It is true to say that this is a trick that relies upon the way the measurement is generally done, but it is very widely used nonetheless. Note that some more recent standards use Peak (PK) detection, which are not 'fooled' by spread-spectrum clocking.

Some devices do not like being driven by spread-spectrum clocks, so take care when using this very powerful technique.

When spread-spectrum was first developed, most wireless broadcasts and communications used fixed-frequency channels, and tests showed that spread-spectrum emissions did have less of an interference effect in line with their reduced QP and AV measurement results. But most wireless is changing to use digital frequency modulation (e.g. GSM, Wi-Fi, Wi-Max, digital TV, Digital Radio Mondiale, etc.) and there are some indications that the emissions from spread-spectrum clocking cause more interference than those from fixed-frequency clocks.

- *Choosing clock frequencies.* When using multiple clocks in a product, try to avoid having any of their fundamental or harmonic frequencies within 500kHz of each other, taking initial tolerances, ageing and temperature variations into account. The normal variation between clocks of the same nominal frequency might not give sufficient variation, especially if they can all 'lock-up' due to EM coupling within the product. See pages 11-6 and 11-7 of [10] for more on this.
- *Driving crystal oscillators.* The crystal circuit has a high impedance at its desired oscillation frequency, but if driven with a square-wave by the associated IC it can have a low impedance at some of the harmonic frequencies, leading to increased levels of emissions. So always check crystal oscillator waveforms, and if they don't look like nice sine waves add some series resistance in series with the IC's crystal drive output.
- *25% duty-cycle clocks.* Ordinary clocks use a 50% duty cycle (1:1 mark:space) but a 25% duty cycle has about half of the spectral amplitude. Where this technique can be used, it should reduce emissions by about 6dB (all else being the same).
- *Optimal Spectral Diffusion (OSD)* [12]. This clocking technique claims to be much better than spread-spectrum, without the problems with certain types of devices. The author has no experience of it.

1.2 Demodulation and intermodulation

1.2.1 The problem

Demodulation and intermodulation happen in all semiconductors, and all the pins on ICs or other semiconductor devices can be susceptible. Once radio frequencies get into a semiconductor device, it is very difficult to predict where they go and which of the transistors and diodes inside the device they might upset. This is a problem for all analogue and digital ICs. But it is more commonly a problem for analogue circuits because digital circuits have inherent noise immunity (noise margin) when they are well designed, whereas analogue circuits do not.

In analogue devices, demodulation and intermodulation (at levels too low to cause actual damage) cause errors in circuit behaviour, or performance degradation (e.g. an increased noise level), but at least they usually recover once the source of the interference is removed.

However, when demodulation or intermodulation effects exceed logic thresholds, state machines and software can go wrong in such a way as to make a product malfunction or else be completely useless, even when the interfering source is removed, until the product is restarted.

Figure 1D shows the results of a real-life radiated immunity test on a small industrial product that used a single device – an LM324 quad operational amplifier (opamp) in an unshielded plastic case. At the time of the measurement, the LM324 (or μ A324) was the lowest-cost quad opamp available in the Far East, and it is quite a slow device, with a slew rate of around 1V/ms and a gain-bandwidth product of around 1MHz.

It is noteworthy that such a slow and low-cost opamp could demodulate at 1000MHz with greater facility than it demodulated at 500MHz. This is fairly typical behaviour for opamps, which will demodulate RF up to many

GHz, although in most larger products the size of the PCBs and wiring and their associated stray capacitances often cause the peak response to RF immunity tests to occur between 200 and 600MHz.

Specifications and standards for immunity testing of ICs are being developed, and in the future it may be possible to buy ICs that have EMC specifications on their data sheets. For now, all we can say is that most bipolar opamps are generally more susceptible to demodulation and intermodulation than most FET or CMOS types, and fully differential (or 'balanced') amplification is generally less susceptible than 'single-ended'. Demodulation is a particular problem for audio circuits in cellphones, where the RF fields from the cellphone's transmitter can be very intense indeed, see Figure 1E. Fully differential ICs have been developed to help overcome this problem [13].

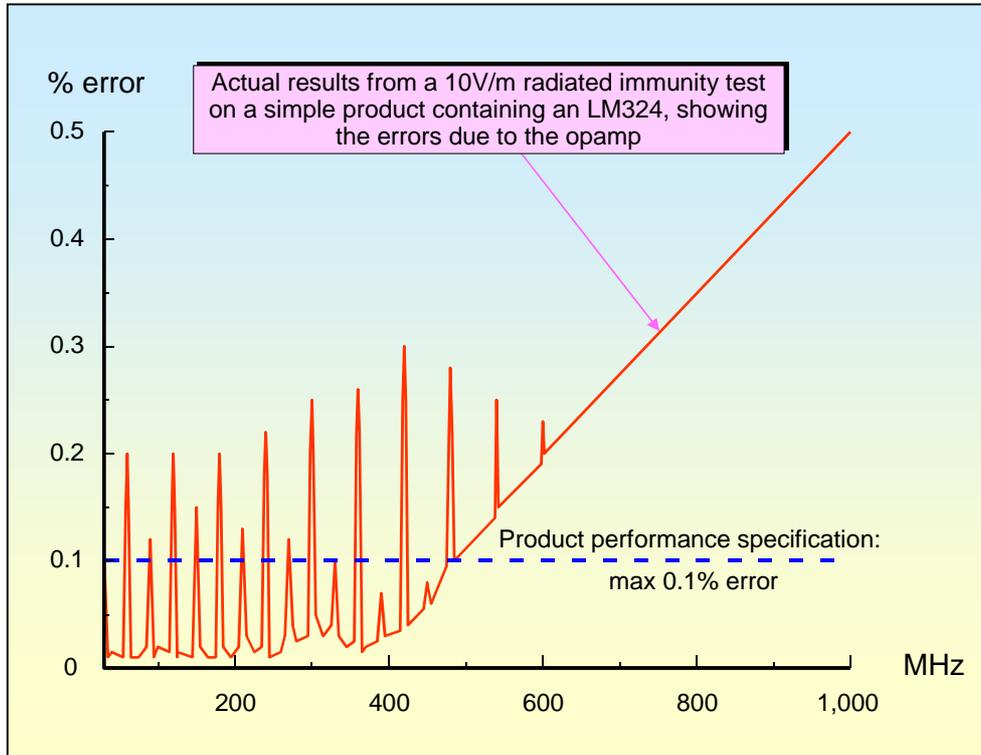


Figure 1D Opamps demodulate radio frequencies very well

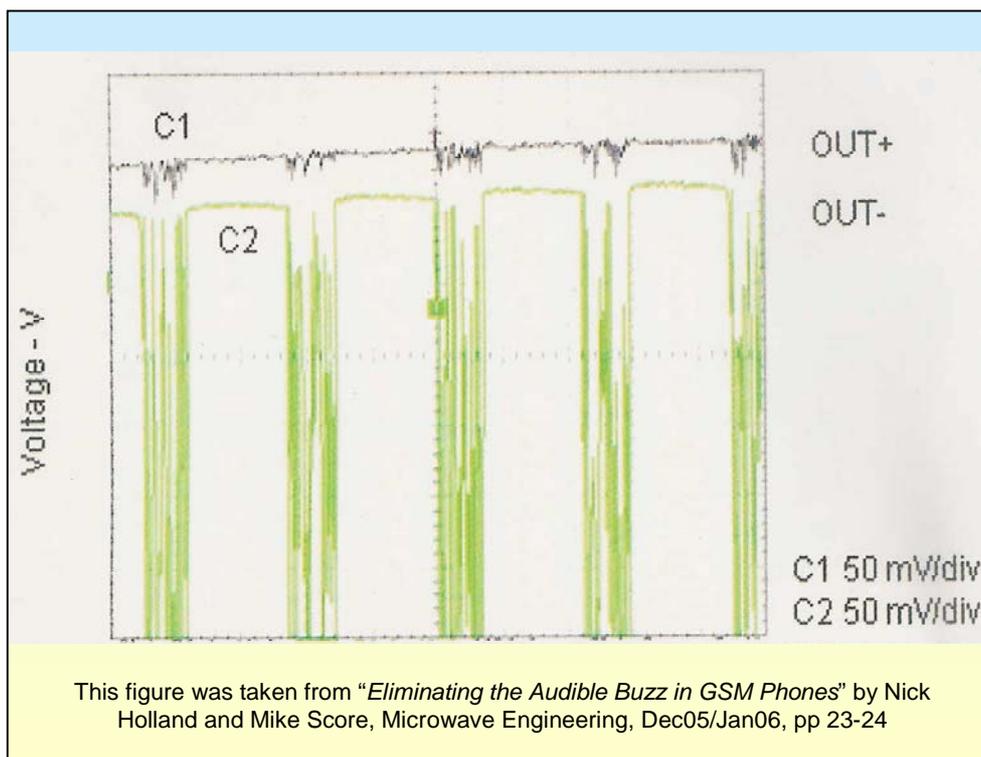


Figure 1E Example of GSM demodulation at the output of a cellphone speaker driver

1.2.2 Designing to prevent demodulation and intermodulation in analogue circuits

To help prevent demodulation and intermodulation, analogue circuits that use feedback need to remain linear and stable when exposed to frequencies outside of their range of linear operation. The solution is to use passive filtering and shielding to ensure that no devices can experience significant levels of frequencies that are above their range of linear operation. Filters and shielding add weight and cost, so to improve cost-effectiveness the circuit should be designed so that the range of linear operation of the devices extends to the highest frequency that can be achieved in serial manufacture.

It is easy to measure the range of linear operation of a feedback circuit using frequency-domain or time-domain methods. Time-domain methods have the advantage of using signal generators and oscilloscopes that most circuit designers will have available, and do not use spectrum analysers. Figure 1F shows one well-proven time-domain method. All inputs, output loads and filters are removed from the circuit and a square-wave test signal injected into the input (outputs and power supplies can also be tested, injecting via small capacitors). The test signal is set to a frequency near to the centre of the passband of the circuit, and it must have a rise/fall time of 1ns or less. Its amplitude set by a 50Ω input attenuator so that the circuit's peak-to-peak output is about 30-50% of the clipping level.

The circuit's input and output signals are then observed with an oscilloscope and probes that achieve at least 100MHz. The input signal is monitored for any deviation from a very fast-edged square wave, and the output signal's slew rate, overshoot and ringing is measured. A 100MHz oscilloscope and probes are required even for audio, instrumentation or other low-frequency or DC circuits. For high-speed analogue circuits use sharper square waves and faster 'scopes and probes, and take very great care to use effective high-speed probing techniques.

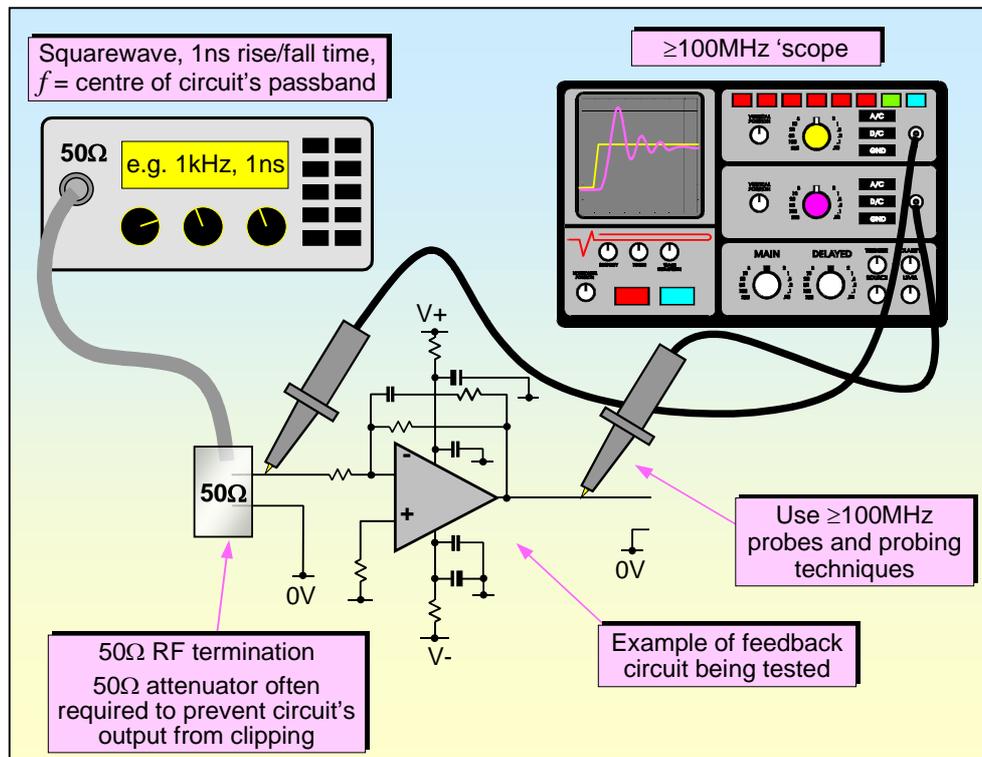


Figure 1F Time-domain testing feedback circuits for stability and linearity

The circuit should be modified as necessary so that – for both the positive and negative going outputs – slew rates are maximised and overshoots are reduced to well below 50%. Any damped ringing longer than two cycles should be reduced, and any bursts of oscillation eliminated. The achievement of these parameters indicates that the linear range of operation has been maximised.

Different batches of ICs can have very different instability performance, most easily simulated by cooling and heating the device under test over a wide range of temperatures (say: -30 to +180°C) whilst ensuring the circuit slew rate remains high and overshoots and ringing are low over the whole temperature range. Circuit modifications are often required to achieve this. Now we have a good circuit to which we must add passive filtering (and maybe shielding), which should both be designed to provide high attenuation at the circuit's ringing frequency and above.

After all this we can add the input cables, output cables and/or loads, power supply, etc., and verify the overall performance using the same test signal. The output should always be a good quality square wave with rounded edges from the filtering, and very little or no overshoot.

1.3 Analogue and data conversion: choosing active devices and circuit design

1.3.1 Choosing active devices

Choosing analogue and data converter components, and designing their circuits for good EMC, is not as straightforward as for digital because of the greater variety of waveshapes, gains, and functions. But as a general rule for low emissions analogue circuits, choose circuit topologies that are good for EMC, and then keep their dV/dt and dI/dt as low as possible (taking device and circuit tolerances, temperature, etc. into account) without compromising functionality. For example, where power efficiency and PCB area are not critical, a linear regulator that has been designed to be unconditionally stable will create no detectable emissions, whereas a DC/DC converter that provides the same functions can easily be a cause of high levels of emissions.

Devices with specified EMC features or performance are preferred (preferably with minimum and maximum specifications, where appropriate), including...

- *Balanced (differential) devices.* These drive or receive antiphase (\pm) signals over two dedicated conductors, and do not use the 0V system for their signals' return current paths. These devices may be able to be used stand-alone, or may require balanced circuits (see below).
- *Separating areas for analogue and digital pins.* Comparators and data converters should have an area dedicated to analogue pins, and an area dedicated to digital pins. Each area should contain the pins for the associated power supply and 0V connections. This is to assist in the segregation of the circuits on the PCB (see Part 5 of this series, Part 5 of [1], or Part 2 of [3] for more detail), which should still be done even when a common 0V plane is used for both the digital and analogue areas (usually required for EMC these days).
- *Data converter digital sections follow digital device guide.* The digital sections of these devices should follow the advice given for digital device selection above, where relevant.
- *Devices that have EMC application notes.* But always check that the guidance follows modern good EMC practices – such as those described in this series.
- *Grounded metal lids.* Where a ceramic-bodied device has a metal lid, the lid should be connected internally to the 0V pin.
- *Beware very fast devices.* There are operational amplifiers and comparators available with very large gain-bandwidths and/or very high slew rates. These require the use of RF design techniques to be made stable, and if they are not stable they can create EMC problems. So only use such fast devices if they truly are necessary.
- *Low A-D converter 'back-fire' noise.* Analogue to digital converters output a small amount of charge into their analogue inputs each time they sample or perform other operations on the input signal. Quite apart from the fact that this transient noise can affect the amplifier or source supplying the signal to the converter, causing errors, if this current flows in a long conductor it can cause problems for EMC emissions.
- *Low D-A converter output noise.* Digital to analogue converters output a small amount of charge into their analogue outputs each time they change they perform a conversion. Quite apart from the errors this transient noise can cause in the reconstruction amplifier, if this noise current flows in a long conductor it can cause problems for EMC emissions.

1.3.2 Analogue and data converter circuit design

- *Ensure unconditional stability.* It is very important indeed for EMC that devices and circuits do not become unstable (e.g. excessive ringing at their outputs) or burst into oscillation. This is a big problem for feedback designs (including voltage and current regulator circuits), but it is also a problem for devices such as comparators and data converters, due to 'accidental' feedback around the circuit, caused by stray capacitances and/or inductances.

Stability testing techniques, such as the one described above in the section on demodulation and intermodulation are very important, and should take into account the full range of device and passive component parameter tolerances and ageing, and the effects of temperature.

Some linear regulators have a tendency to self-oscillate under certain load conditions, so their stability should be tested over the full range of their likely load currents and inductive/capacitive loads. Instead of the pulse generator in Figure 1F, the stability can be tested with a signal generator driving a transistor that switches a load in or out of circuit. The rate of switching can be low (e.g. 100Hz) but the rise/fall time of the load must be less than 1 μ s.

- *Avoid clipping.* Driving an amplifier stage into clipping creates harmonics of the signal being clipped, and these can cause great problems for EMC (and also for meeting the transmitter radio spectrum control requirements of the R&TTE directive and similar regulations). Even low-frequency signals can have RF emissions when they are clipped.

Some types of circuits (such as audio amplifiers in professional and musical applications) are regularly driven into clipping during use, causing interference problems that are not evident from the normal tests (which use unclipped signal levels). Where clipping is likely in use, and where 'soft-clipping' circuit techniques have not been used, the circuits should be tested with typical clipped signals.

- *Avoid instability due to clipping.* Another problem with clipping is that while it is happening, feedback circuits suffer very large error voltages at their summing points. These can drive devices into operating areas in which their gain or phase can shift, causing the circuit to become unstable. This can easily be checked by using a fast oscilloscope (and appropriate probes and probing techniques) to observe the unfiltered output waveform as the circuit comes out of clipping. There should be no ringing or oscillation or visible distortion of the waveform – the circuit should exit 'cleanly' from its clipped condition. Instability during clipping can depend on the degree of clipping, so these tests should cover the full range from 'just-clipped' to 'massively over-driven'.
- *Buffer capacitive loads.* Achieving good stability in feedback circuits usually requires that capacitive loads (e.g. cables) be buffered from the feedback circuit by a small resistance or choke.
- *Don't use integrator feedback without a series resistor.* Feedback circuits using integrator capacitors larger than about 10pF generally need a low-value resistor (often around 560Ω) in series with the capacitor, for stability. The resistor stops the circuit from trying to be an integrator when the phase shift through the amplifying device exceeds 90°. This aid to stability may require some reworking of the circuit to achieve the desired time-constants.
- *Take great care with active filters or integrators.* Never try to filter or control RF bandwidth for EMC with active circuits – only use passive (preferably RC) filters outside any feedback loops. At frequencies higher than the open-loop bandwidths or the active devices used, passive filters should always be used, outside of any feedback loops, to control time or frequency behaviour.
- *Matched transmission line techniques.* These help reduce emissions and improve immunity when the highest frequency (f_{max}) of any significance in an analogue signal is greater than $1/(25t_p)$, where t_p is propagation delay along the full length of its conductor (whether a PCB trace, wire or cable). For example, if the propagation time along a PCB trace was 1ns, using matched transmission line design might help reduce emissions from the PCB at frequencies over 40MHz. PCB transmission line design and matching is discussed briefly in the forthcoming Part 5 of this series, Part 5 of [1], and in more detail in Part 6 of [3].
- *Suppress all interconnections.* Having achieved a stable and linear circuit as described above, any and all of its interconnections might need protecting by passive filters or other suppression methods (e.g. opto-isolators). This applies to *all* external interconnections unless they are very well-shielded along their entire route, and may also apply to internal interconnections (within the product) where digital and/or switch-mode converter circuits are also used.

Suppression is covered in the forthcoming Part 3 of this series, and in Part 3 of [1]. The suppressors associated with a device should connect to its PCB's local 0V plane (see the forthcoming Part 5 of this series, Part 5 of [1], and Part 4 of [3] for more detail). Filter design can be combined with galvanic isolation (e.g. a transformer) to provide protection from DC to many GHz. Using balanced (differential) inputs and outputs can help reduce filter size while maintaining good rejection at lower frequencies.

- *Use RF power supply decoupling.* This is needed for all power supplies and voltage reference pins, for stability as well as reducing emissions and increasing immunity. Appropriate decoupling techniques are described in the forthcoming Part 5 of this series, Part 5 of [1], and in more detail in Part 5 of [3].
- *Use LF power supply decoupling.* Analogue devices and the analogue portions of data converters generally need power supply decoupling at lower frequencies than digital devices, because their power supply noise rejection ratio (PSRR) usually 'rolls off' above 1kHz. RC or LC filtering of each analogue power rail at each opamp, comparator, or data converter, may be needed. The corner frequency and slope of such power supply filters should compensate for the corner frequency and slope of device PSRR, to achieve the desired PSRR over the whole frequency range of interest.
- *EMC for RF circuits.* Not many EMC design guides mention RF design. This is because RF designers are generally very good with most continuous EMC phenomena, and their circuits generally use single frequencies or a narrow range of frequencies. Spectrum control requires them to keep emissions of harmonics and spurious noise very low. However, local oscillators and IF frequencies often leak too much, so may need more attention to shielding and filtering.
- *Avoid the use of very high-impedance inputs or outputs.*

- *Comparators must have hysteresis (positive feedback).* This prevents false output transitions due to noise and interference, and also prevents oscillation near to the trip point caused by the stray capacitance between the digital output and the analogue inputs. Don't use faster output-slewing comparators than are really necessary (i.e. keep their dV/dt low).
- *Clock synchronisation.* Where there are analogue functions in the product, especially audio or video, the digital and switch-mode clocks should ideally be all phase-locked together, to prevent heterodyning (intermodulation) causing varying whines or warbles or flickering bars. A single clock synthesiser with multiple frequency outputs might be the best, and 'fractional-N' types are available so that the frequencies do not have to have simple numerical relationships with each other. Interference that still occurs due to clock noise will at least be constant, and it is sometimes possible to arrange for it to occur in periods where it doesn't matter, e.g. during the hold time of a sample/hold circuit, or during the blanking period of a video picture.
- *Use balanced (differential) circuits.* Balanced ('differential') circuits drive antiphase (\pm) signals over two dedicated conductors, and do not use the 0V system for the signal's return current path. Common-mode (CM) voltages and currents cause most of the emissions from products, and most environmental EM threats and immunity tests are also CM – so using balanced send and receive interconnection techniques ('differential signalling') has many advantages.

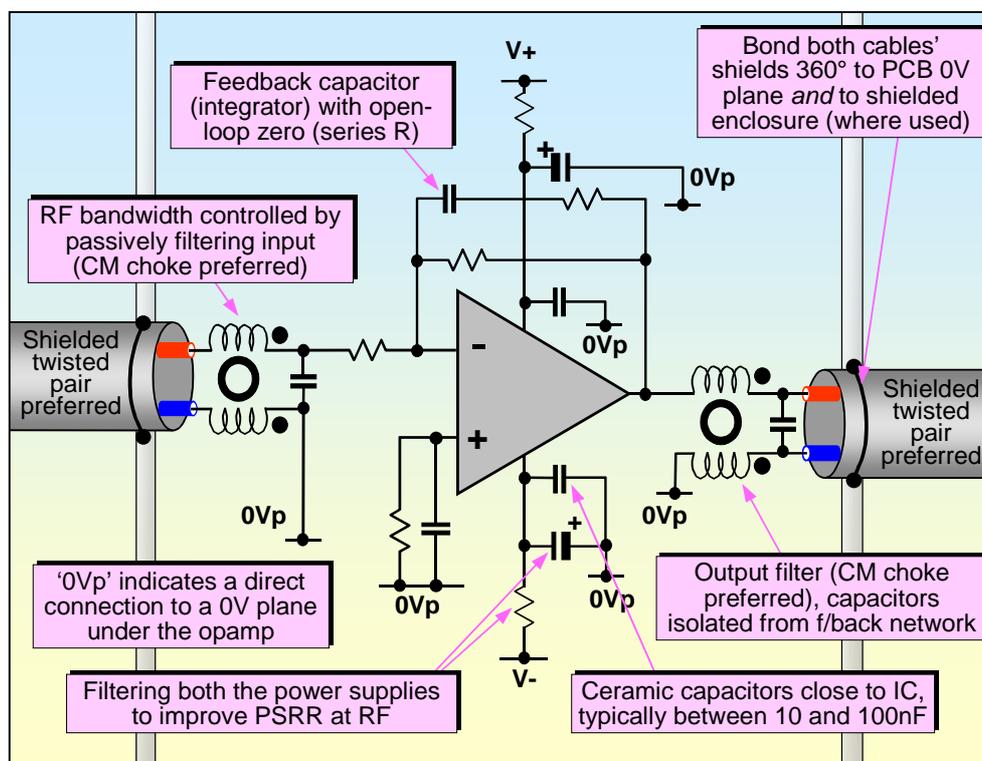


Figure 1G Example of a simple analogue circuit

Figure 1G shows a simple single-ended opamp circuit (an inverting amplifier) with some of the circuit techniques mentioned above applied.

Even though the circuit does not use differential signalling (i.e. it uses 0V as the common for its signal returns), CM chokes will generally improve the EMC performance when used in the input and output filters.

Suppression is generally needed for all external cables, unless they are very well shielded along their entire length (including their connectors and the circuits at both ends). Wired interconnections inside unshielded enclosures may also need suppressing, as might wired interconnections inside any enclosures that contain digital processing or switch-mode power converters.

Suppression is often required where analogue devices connect with data converters or clocked digital devices, but not generally required if they connect to other analogue devices by means of PCB traces routed over a 0V plane used by both of their circuits.

For more detailed advice on analogue circuit design, see [14].

1.4 Switch-mode power converter design

Switch-mode power conversion technologies include AC-DC conversion (e.g. off-line DC power supplies), DC-DC conversion (e.g. generating multiple DC voltage rails from a single voltage supply) and DC-AC conversion (e.g. inverters). A mains-powered inverter (e.g. a variable speed drive for an induction motor, or a so-called 'electronic transformer' for low-voltage domestic lighting) consists of an AC-DC converter followed by a DC-AC converter.

Switch-mode power conversion is inherently electrically noisy, and can easily produce very high levels of emissions (typically up to 1,000 times the switching rate) if not carefully designed using the techniques described below. These techniques can also help make switch-mode power supplies have sufficiently low noise to power sensitive analogue circuits.

1.4.1 Circuit topology

Always switch voltages or currents softly, rather than abruptly: keep both dV/dt and dI/dt as low as possible at every instant throughout each switching cycle. There are a number of circuit topologies that reduce emissions by reducing dV/dt and/or dI/dt , whilst also reducing the stresses on the switching transistors. These include ZVS (zero voltage switching), ZCS (zero current switching), Resonant mode (a type of ZCS), Quasi-resonant mode, SEPIC (single-ended primary inductance converter), Cük (an integrated magnetics topology, named after its inventor), etc.

The choice of active devices depends very strongly on the choice of the circuit topology. Many types of controller IC only suit one topology.

It is important for low emissions that continuous-mode topologies don't ever operate in discontinuous mode, and that discontinuous-mode topologies don't ever operate in continuous mode. It is also important that control loops are stable at all times.

Avoid 'pulse-skipping' converters, and beware of 'stand-by' modes of operation that produce much higher levels of emissions than when the converter is running normally.

1.4.2 Soft-switching

Some switch-mode designers seem to think that the shortest switching times are always the most efficient. But when using traditional circuit topologies, where the power devices are not switched at zero volts and/or zero current, it is not true to say that reducing switching time always leads to better efficiency. The inevitable RF resonances of the circuit's components (especially the wound ones) requires increasingly lossy snubbing to protect the power switches from overvoltages as switching times decrease, and for switching times below a certain critical value overall efficiency will worsen.

Shorter switching times means more energy in higher-frequency harmonics, in the same way as was shown for digital devices by Figure 1A, requiring more costly EMC measures. In poorly designed switch-mode power converters, harmonics of up to 1000 times the basic switching rate often cause failure to meet emissions tests.

So a degree of soft-switching is generally required to achieve the most cost-effective overall design that takes into account the costs and sizes of filtering and shielding required to comply with EMC requirements. In some cases the best cost-effectiveness might require the efficiency to be one or two percent below the best achievable. In small DC/DC converters, all that may be needed is a resistor of 100Ω or so in series with the switching FET's gate to reduce the conducted and radiated emissions dramatically, with no appreciable extra heating.

For a power switching FET, the rate of change of drain voltage is a non-linear function of its gate voltage. Using the 'gate charge model' (which includes the 'Miller effect' from C_{dg}) can help achieve gate drive circuits that control the drain's dV/dt so as to generate lower emissions for the same overall switching time.

1.4.3 Preventing self-oscillation

Switching devices, especially power FETs, can self-oscillate, causing high levels of emissions and sometimes overheating too. This is especially a problem where power FETs are paralleled to handle higher currents. Driving the FET gates via low-value resistors, or small soft-ferrite RF suppressor beads can generally cure it. Each resistor or bead must be located *very* close to the power FET's gate terminal.

The problem can also arise when Schottky diodes are paralleled, in which case ferrite beads should be connected in series with one or more of the devices.

1.4.4 Spread spectrum and random modulation techniques

'Spread-spectrum clocking' techniques can be used with some switch-mode topologies to spread the emissions spectrum of the individual harmonics so that they measure less on an EMC test. Commercial and industrial

conducted emissions tests use a 9kHz bandwidth from 150kHz to 30MHz, so spreading a harmonic by $\pm 90\text{kHz}$ can give reductions of more than 10dB. Some high-power converter manufacturers use almost white noise. See [15] and [16] for more on this technique.

1.4.5 Snubbing

Snubbing is usually required to protect the switching transistors from the peak voltages produced by the resonance of stray elements in the circuit components.

Figure 1H shows how the stray leakage inductance and inter-winding capacitance typical of a winding, such as in an isolating transformer, create a parallel-resonant circuit. The resulting high impedances at resonance cause the currents that are trying to flow at those frequencies to create large voltage overshoots. The more abruptly its current is switched, the more energy there is at or near the resonant frequencies, and the higher the overshoots and resulting emissions.

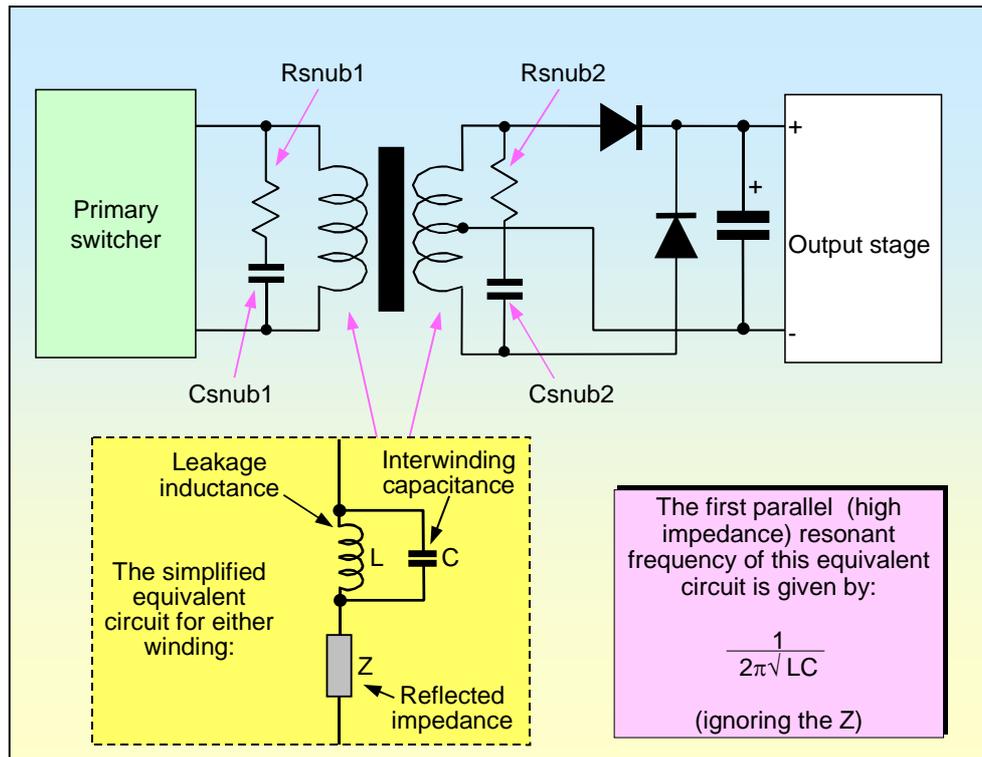


Figure 1H Snubbing in switch-mode converters

Snubbers are generally best connected across switching devices – so as to account for the inductance and capacitance of their interconnects too. There are many possible types of snubber designs – the resistor and capacitor in series (RC) type shown in Figure 1H is the simplest to design and usually the best for EMC, but it can run hotter than other types, wasting more power and reducing overall efficiency, so be prepared to compromise.

Snubbers should be designed and realised in actual assembly in such a way as to minimise their inductance. Devices, passive components and conductors should have very low-inductance, so special low-inductance power resistors may be required, and pulse-rated capacitors should be used, with very short leads to the device concerned.

1.4.6 Reducing emissions from heatsinks

A TO247 power device with an insulating heatsink washer has around 50pF of stray capacitance between its collector (or drain) and its heatsink, and similarly-sized device packages have similar stray capacitances. These stray capacitances cause the dV/dt of the collector (or drain) to inject a transient current into the heatsink on every switching operation. If the heatsink is not connected to anything (i.e. is 'floating') the resulting dV/dt of the heatsink can be almost as great as that of the device's collector (or drain), and the large size of the heatsink then creates strong emissions of electric fields.

If instead the heatsink is connected to part of the circuit, 0V, or chassis, the transient injected currents will flow through it into the circuit, 0V or chassis. If this current path is not controlled correctly it can cause conducted emissions problems, as well as emitting electric and magnetic fields.

It is usually best to connect primary switching device heatsinks directly to one of the primary DC power rails – taking full account of all safety requirements, which might require a clear hazard warning on or near the heatsink, for the sake of design engineers and maintenance personnel. Switchers operating on isolated secondary voltages should generally have their heatsinks connected to one of the secondary DC rails, or to the local 0V plane. The loop area enclosed by the transient currents (see Figure 1J) should be as small and low-impedance as possible. Always perform some iteration on a prototype to find which rail it is best to connect the heatsink to.

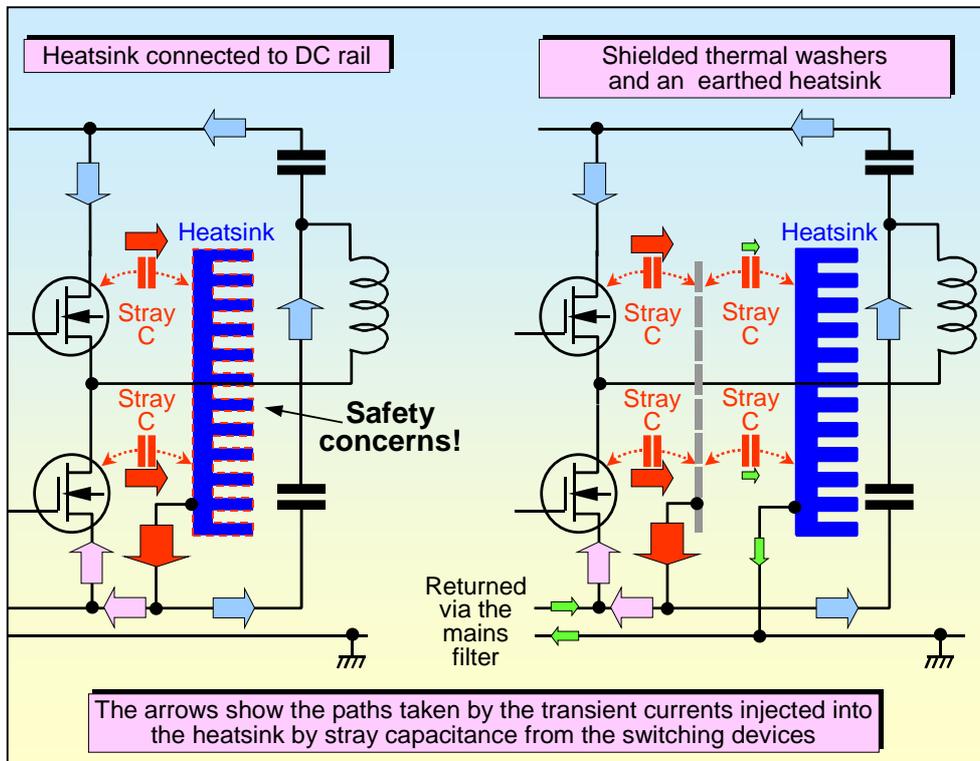


Figure 1J Controlling the paths taken by transient currents due to device stray capacitance

Sometimes switching devices are mounted on heatsinks without insulating thermal washers, to save money or reduce thermal impedance. Where heatsink isolation is not provided inside the device itself, the heatsink is connected to the collector (or drain) and it is then impossible to connect it to the appropriate power rail. The solution here may be to connect the heatsink to the rail via a suitably-rated capacitor. The author has seen this technique used to great effect when the noise source was the heatsink tab of a T0-220 switching device, with no additional heatsink. A few pF of capacitance was all that was required to reduce E-field emissions by more than 30dB.

Another reason for using a series capacitor might be to reduce the mains leakage current that can occur should someone accidentally touch the heatsink, for safety reasons. When using a series capacitor, it might be possible to ‘tune’ the capacitance with the inductance due to the length of its leads and other interconnecting conductors – using series (low-impedance) resonance filter to minimise the most troublesome band of frequencies.

Where such ‘heatsink-RF-bonding’ capacitors are associated with safety issues, as they often are, they should be of a suitable value, rating, and construction (e.g. Y1 or Y2) having regard to the requirements of the relevant safety standard(s). The author also recommends that such capacitors are approved for their maximum voltage and application by an independent safety agency (e.g. BSI, TUV, VDE, SEMKO, DEMKO, UL, etc.) and their approval certificates obtained and checked with the issuing agencies to ensure that they are not forgeries.

An alternative is to use shielded thermal washers. Their shielded inner layer is connected to the appropriate DC rail, while the heatsink itself can remain isolated or else be connected to some part of the circuit, 0V or chassis, in which case the small remaining heatsink currents are eventually returned via the mains filter. Although this is safer, it is more costly and might not give as good EMC performance due to the transient currents in the 0V or chassis.

1.4.7 Reducing emissions from rectifiers

Rectifiers can cause a great deal of noise (hence emissions) due to the transient currents that flow when the voltage across them is reversed during the switcher’s cycle. This is true even for mains rectifiers, which have been seen to emit excessive emissions at several MHz.

Mains rectifiers can usually be suppressed with a small capacitor connected in parallel with each device, and the rectifiers in switch-mode converters can sometimes use snubbers to help suppress their noise. But the best solution is to use Schottky rectifiers instead of ordinary PN junction types. Schottkies have no minority carriers, hence no reverse current, hence no transient currents and noise upon voltage reversal. Now that high-voltage silicon-carbide Schottkies are available, there are fewer restrictions on where Schottkies can be used.

Another alternative is to use synchronous rectification, replacing or paralleling the rectifier with a switching device such as a power FET. Synchronous rectification is usually done to improve efficiency, but often has EMC problems caused by the parasitic PN junction rectifiers inherent in the switching devices.

If using PN junction rectifiers, for good EMC they need to be types that have very small stored charge, and 'soft switching' so that they do not excite the resonances in the circuit's components, as shown by Figure 1K.

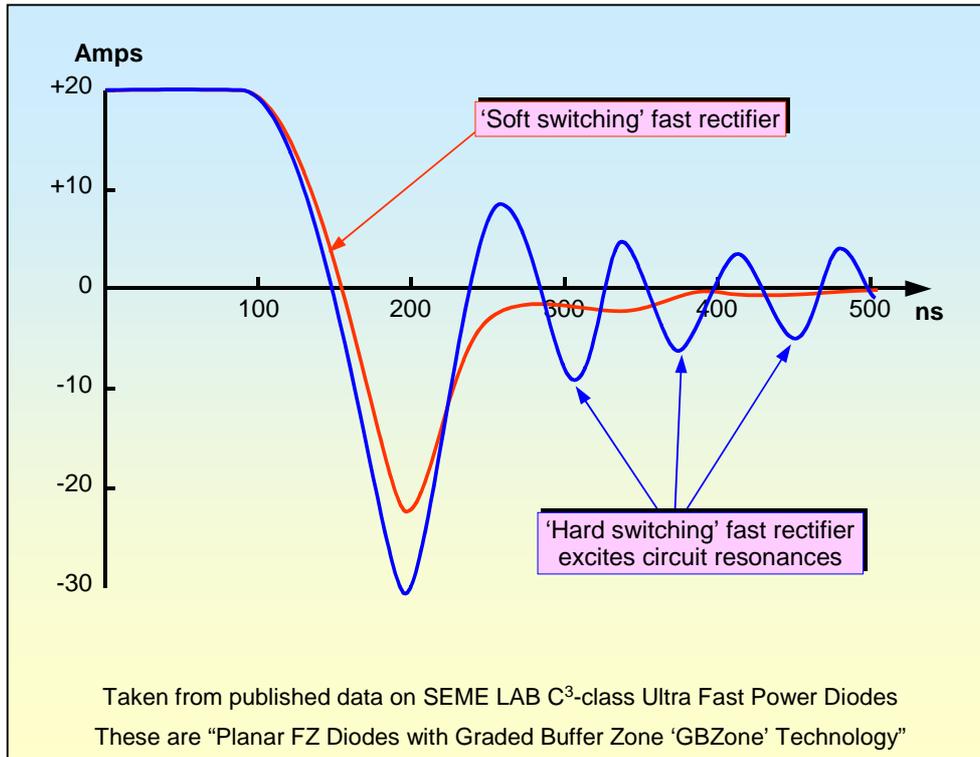


Figure 1K Rectifier noise reduced by using 'soft-switching' devices

'Amorphous beads', which look like ferrite beads, can be slipped over the lead of a rectifier to make its reverse recovery 'softer' and reduce emissions. See pages 10-10 and 10-11 of [10]. Resistors and 'ordinary' ferrite beads may also be able to be used for this purpose.

According to [17] if switching FET's source and drain currents are both passed through a small *saturable* inductor bead it can help control di/dt and hence allow the use of cheaper, lower-spec rectifiers. This technique also requires modifications to the FET's gate drive.

1.4.8 Reducing emissions due transformer interwinding capacitance

Primary switching noise is injected through the stray interwinding capacitance of isolating transformers, creating CM noise in the secondary circuits. And the secondary circuit's switching noise is injected in the opposite direction, via the isolating transformer's interwinding capacitance, and this appears as a CM noise in the primary circuit. These CM noise currents have a high source impedance and are difficult to filter. They travel long distances – enclosing large loop areas where necessary to satisfy Mr Kirchoff's famous law, thereby creating significant emissions problems.

Interwinding shields can help reduce this noise, and should be connected to the DC rails on the sides whose noise it is desired to reduce. Two or three interwinding shields may be needed to reduce the primary and secondary noise injections by enough, and five shields is not unheard of. When using an odd number of shields, the shield in the middle might benefit from being connected to the chassis, 0V or protective earth.

Figure 1L shows an example of a single interwinding shield. Experiments with a prototype are usually needed to find the optimum places to connect the shields to. The shield's interconnections should be as short as possible to reduce their impedance at RF and hence improve their noise reduction.

So-called 'PCB-transformers' are becoming increasingly popular, in which the windings are simply printed traces on different layers of the PCB. Adding shields to these is simply a matter of adding more PCB layers,

whilst ensuring that the necessary clearances are achieved for reliable operation and safety, despite tolerances in PCB manufacture.

Another powerful technique shown in Figure 1L is to provide a local return path for the noise currents with small (safety approved!) capacitors connected between the secondary 0V and one of the primary power rails.

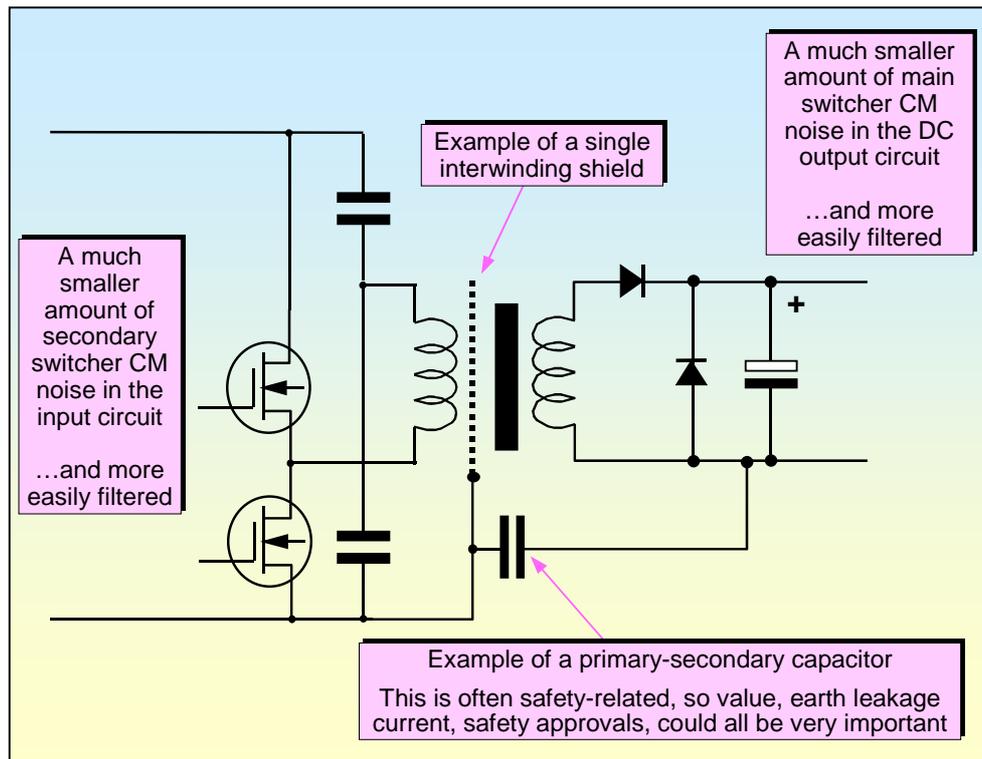


Figure 1L Two remedies for the noise injected by interwinding capacitance

Make sure that the capacitor connected from primary to secondary does not cause the total earth leakage current to exceed the specification in the relevant safety standard. These capacitors also help any primary or secondary filters to achieve greater suppression, by reducing the source impedance of the emissions so that CM chokes can be more effective.

Other aspects of the design of switch-mode isolating transformers can have a large effect on emissions, as described in [18].

1.4.9 Reducing emissions due to transformer or inductor core conduction

Ferrite materials are not insulators, so the stray capacitance from the windings injects pulses of charge into the core in each switching operation, and these flow out of the core as a transient noise current into whatever the core is fixed to. If the core is 'grounded', the transient current has a long way to flow to complete its loop, so tends to cause conducted and radiated emissions.

This is a similar problem to that of heatsink transient currents discussed above, and the solution is similar – either connect the transformer core to the appropriate DC rail (taking care of any and all safety issues), or wrap a shield around the core and connect that to the appropriate DC rail instead.

1.5 Communications circuits

The devices used for communications are either digital or analogue, so their selection should take into account the relevant guidelines described earlier.

1.5.1 Avoid using metal conductors

The best communications for EMC purposes are infrared or optical, via free-space (e.g. IRDA) or fibre-optics. Gb/s data rates are available using laser devices, using either free-space or fibre propagation. The transmitters must not have excessive emissions, and the receivers must be immune enough, but these are small devices and their EMC is usually easier to control than that of a long cable. Shielded transmitters and receivers are now readily available.

Most designers automatically assume fibre-optics will be too costly, but plastic fibre-optics at up to 25Mb/s are now being used in large volumes in motor vehicles, driving down the prices of these components (£4.50 for a 25MB/s TX/RX pair in mid-2004). And don't forget what was said in Part 0 above – the lowest profitable selling

price and the one that will maximise the return on investment over the sales life of the product are generally independent of the BOM cost.

It is often practical to take metal-free fibre-optic cables right through the walls of shielded enclosures to PCBs or modules inside, without compromising the enclosure shielding (whereas metal conductors should always be filtered and/or 360° shield bonded at the points where they enter shielded enclosures, see the forthcoming Part 4 of this series, or Part 4 of [1]).

Free-space optical communications may be an appropriate technique, using line-of-sight lasers or more forgiving infra-red. Wireless communications are another good alternative, but their transmitters can sometimes interfere with nearby electronics (depending on transmitter power and proximity) and their receivers can sometimes suffer from interference, so these issues should be taken into account if they are not to create more problems than they solve.

Another reason for using metal-free fibre-optics, free-space optics (e.g. infra-red) or wireless communications is the automatic achievement of galvanic isolation to very high voltages. This often greatly improves product reliability, reduces warranty costs, and avoids the cost, weight and space requirements of filters, surge protection devices, shielding, etc.

Wires and cables may appear at first sight to be the most cost-effective interconnections, but by the time their EMC problems have eventually been solved at the end of a project – the non-metallic alternatives would sometimes have resulted in lower costs overall and shorter timescales.

Wires and cables are usually cost-effective within a product's fully shielded enclosure, but even then 'intrasystem interference' problems (one circuit interfering with another inside the product) and the slower propagation velocity in cables can make infra-red, free-space or fibre-optic techniques more attractive.

1.5.2 Good EMC practices in communications using metal conductors

Figures 1M, 1N and 1P outline some examples of bad, better, good and excellent practices in communications, using the example of a 0-10mV transducer connected to a remote circuit by a long cable.

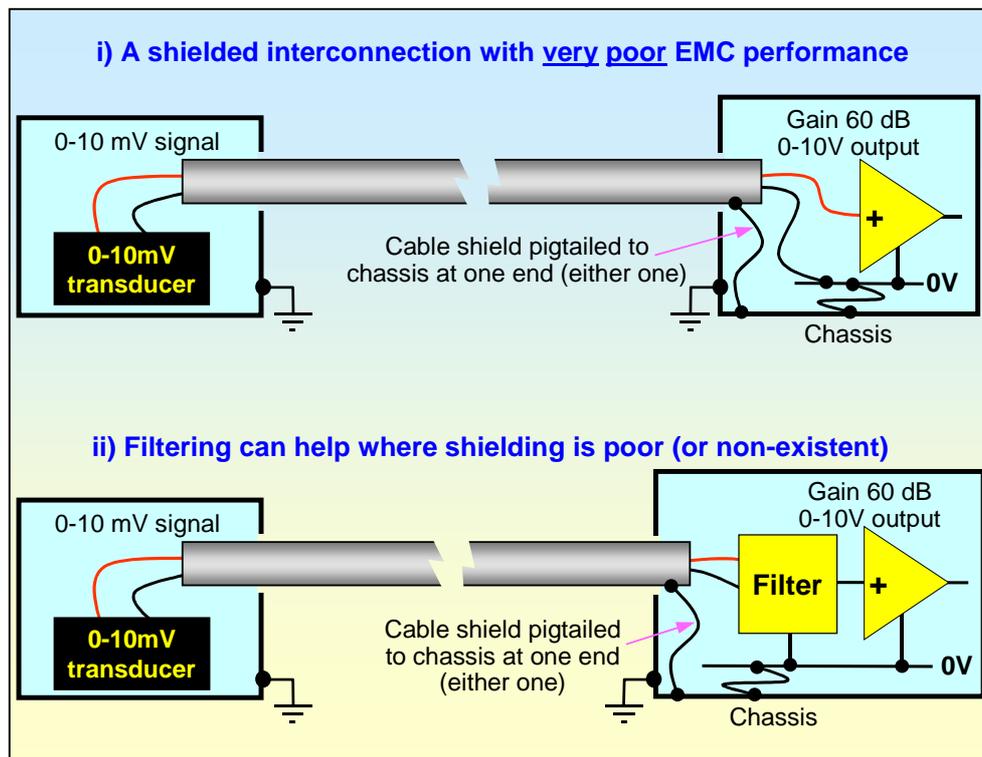


Figure 1M Examples of good and bad practices in signal wiring

In general, connecting a cable's shield to a circuit's 0V is very bad practice for EMC, as is the use of pigtailed and grounding cable shields at one end only. Some textbooks still separate cables into low and high frequency types, with different shield-bonding rules for each. But the EM environment is now so polluted with RF up to 2.45GHz (and getting worse all the time) that almost all signals can be expected to suffer from RF noise, so all cables should now be treated as high-frequency types to control EMC.

Figures 1M to 1P show cable shields that are terminated at both ends, with the note that a PEC (Parallel Earth Conductor, according to [19]) should be used if necessary. This topic, and why the resulting 'ground loops' or

'hum loops' need not be a problem, up to the very highest level of signal/noise performance, when circuits are designed correctly, is covered in the forthcoming Part 2 of this series, and Part 2 of [1].

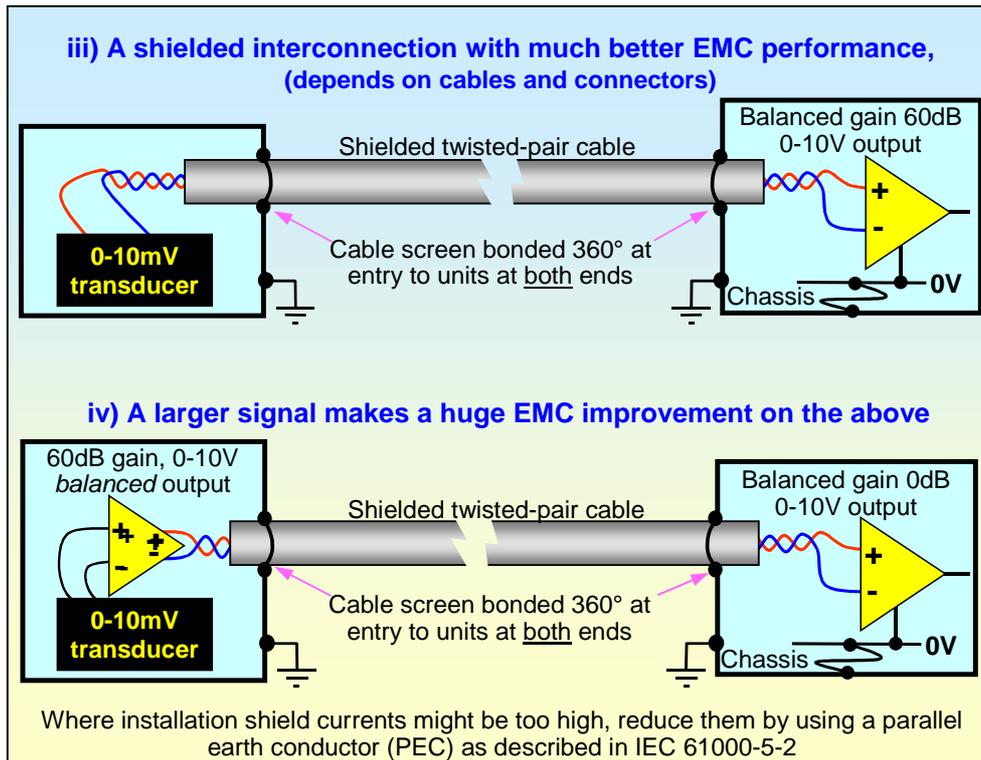


Figure 1N Examples of good and bad practices in signal wiring (continued)

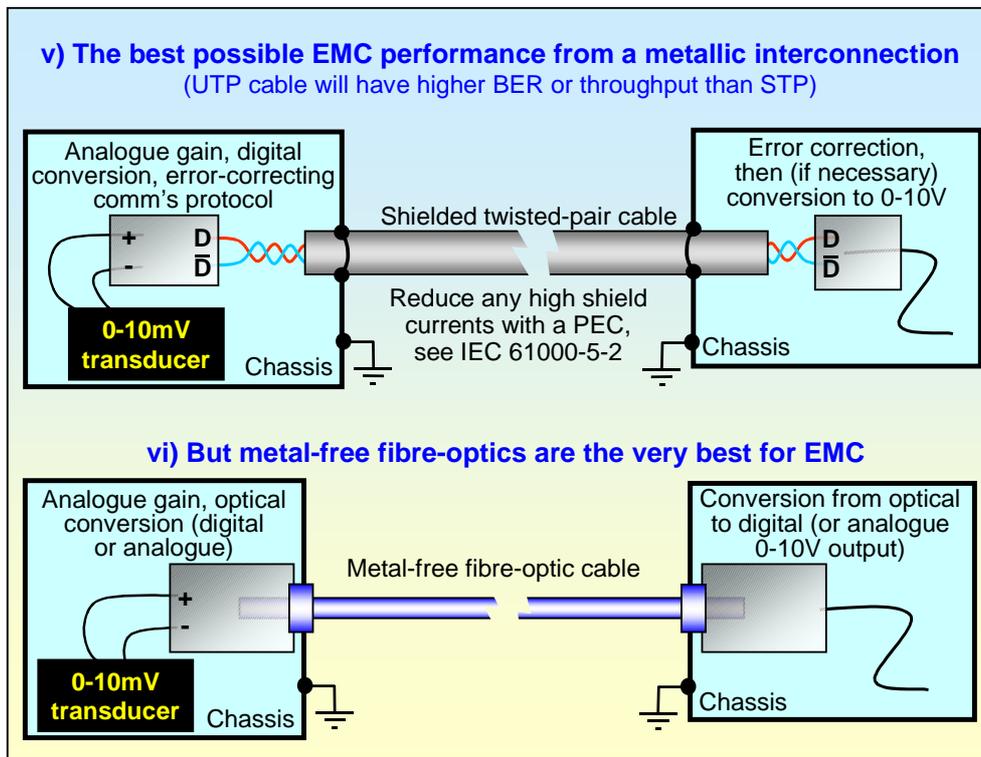


Figure 1P Examples of good and bad practices in signal wiring (continued)

For low frequency signals (say, under 10kHz) – the higher the voltage in the communication link the better, for reasons of immunity. But for high frequencies (say, above 1MHz) lower voltages are preferred for reasons of emissions. Most of the highest-speed data communications now use LVDS techniques (Low Voltage Differential Signalling) that have signal levels between 300mV and 1V peak-to-peak.

Communication protocols for improving immunity. Sophisticated error detection and correction protocols can considerably improve the immunity of a communication scheme. Some protocols (such as Ethernet) reduce

their data rate the more they are interfered with – so although no bad data gets through and the Bit Error Rate (BER) remains very high, the data throughput rate can fall to zero. Communication protocols that do not reduce their data rate if they suffer from interference are available, and may be preferable in some situations. Do not even *imagine* that you or your team can design a communications protocol that will give good immunity – even after many tens of man-years of development what you have designed will not be as good as protocols that are already commercially available.

Embedded clocks. Where a clock needs to be sent across a communication link, it should be embedded in the data to reduce its emissions. A variety of clock-embedding methods have been well-proven, such as Manchester encoding. Manchester encoding also transfers one bit on each data edge, so halves the data rate in the communications medium for a given ‘real’ data rate, which helps reduce emissions too.

Communication protocols for improving emissions. Start and end delimiters, framing and synchronisation bit patterns, token bit patterns, and access control protocols can all have a major influence on how much emitted energy is concentrated into narrow spectral bands during various operational states (high/low traffic, idling, etc.). Appropriate design of the communications protocols should ensure that highly periodic waveforms are always avoided.

Techniques are available (and are used in Gigabit Ethernet) to almost totally randomise data, so that it has no strong spectral components. The emissions are then spreading out across the frequency range instead of being concentrated at specific frequencies.

Matched transmission lines. Transmission line techniques may be essential for good EMC for high-speed analogue or digital signals, depending on the length of their connection and the fastest rise/fall time or highest frequency that will be sent over the cable (see the forthcoming Parts 2 and 5 of this series, or Parts 2 and 5 of [1], and Part 6 of [3] for more detail). It is often not appreciated that the immunity of low-frequency signals may be able to be improved by using matched transmission lines for their interconnections.

The best type of metal cable for EMC purposes usually has a dedicated return conductor twisted with each signal conductor, and a shield that is used only to control interference (not to carry signal return currents). Co-axial cables are generally not preferred for EMC reasons, despite their widespread use by RF engineers and in EMC test laboratories.

Balanced interconnections. Balanced construction twisted-pair or twin-axial cables, or closely-spaced pairs of PCB traces, usually give the best and most cost-effective emissions and immunity performance. For cables, very small differences in twist rate (and even a small difference in the dielectric constants of the pigments used to colour the insulation) can be important for balance at high frequencies. Similar problems affect the balance of differential trace pairs in PCBs (see Part 6 of [3]). Balance is so important that in high-performance circuits a balanced (mirror-image) PCB layout can sometimes be necessary for the devices and their passive components and traces.

It is very important to achieve a good differential balance over the whole frequency range, as this means a good CM rejection ratio (CMRR) and hence improved emissions and immunity. Balanced send/receive ICs are good, but isolation transformers have the benefit of adding galvanic isolation (up to the point where they flash-over) and also extending the CM voltage range well beyond the DC supply rails.

Transformers and balanced send/receive ICs all suffer from degraded balance at RF. They generally require a CM choke to maintain good balance over the whole frequency range of interest, as shown in Figures 1Q and 1R. The CM choke always goes closest to the cable or connector at the boundary of the product.

Figure 1Q shows two examples of circuits that are equally useful for providing good emissions and immunity for digital or analogue communications of any speed or frequency range. These circuits are ideal because they are balanced throughout. Although shielded twisted pair (STP) cable is shown, unshielded twisted pair (UTP) cable could be used but would have worse EMC performance.

Figure 1R shows how the CMRR of the CM choke is tailored to suit the transformer or balanced IC to achieve a good balance (high CMRR) over the whole frequency range of concern.

An alternative type of CM choke is the ‘CM transformer’ shown in Figure 1S. An inductor of sufficient value connected between a pair of differential signals has a high impedance to the signals, but if its centre-tap is ‘grounded’ it presents a very low impedance to any CM signals superimposed on the differential pair. By centre-tapping one side of the isolation transformer in Figure 1S, it has been made to provide both galvanic isolation and a CM filtering effect. When capacitors are used in series with the centre-tap, their resonances (see later) can affect the performance of the CM transformer.

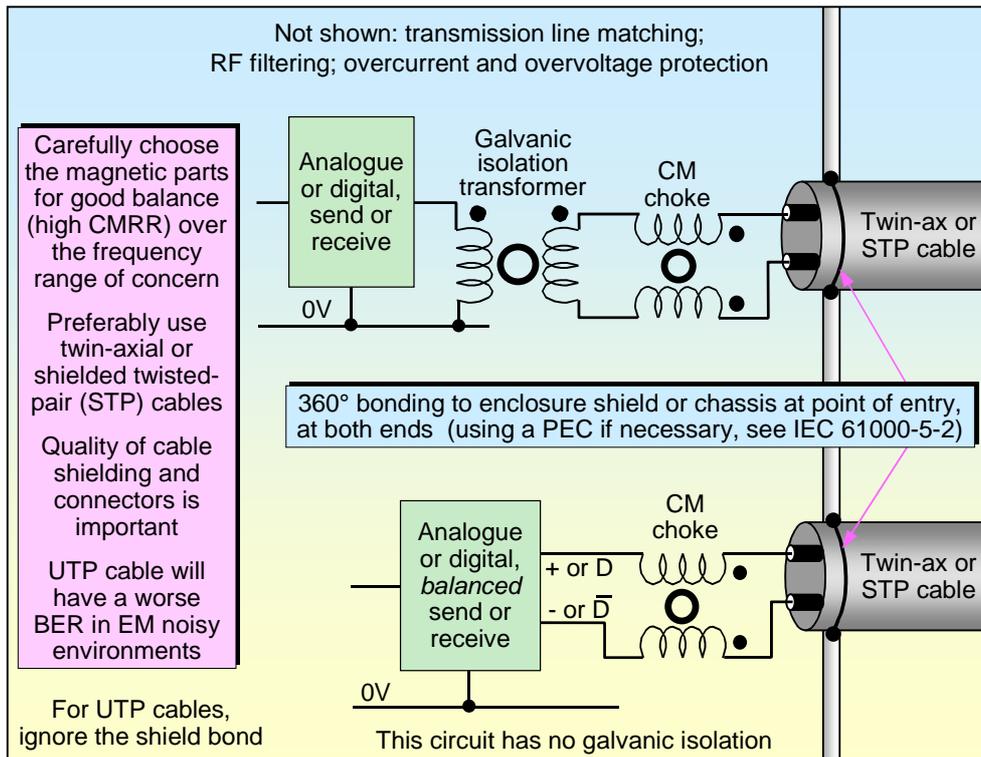


Figure 1Q Examples of good circuits for high-speed signals or data

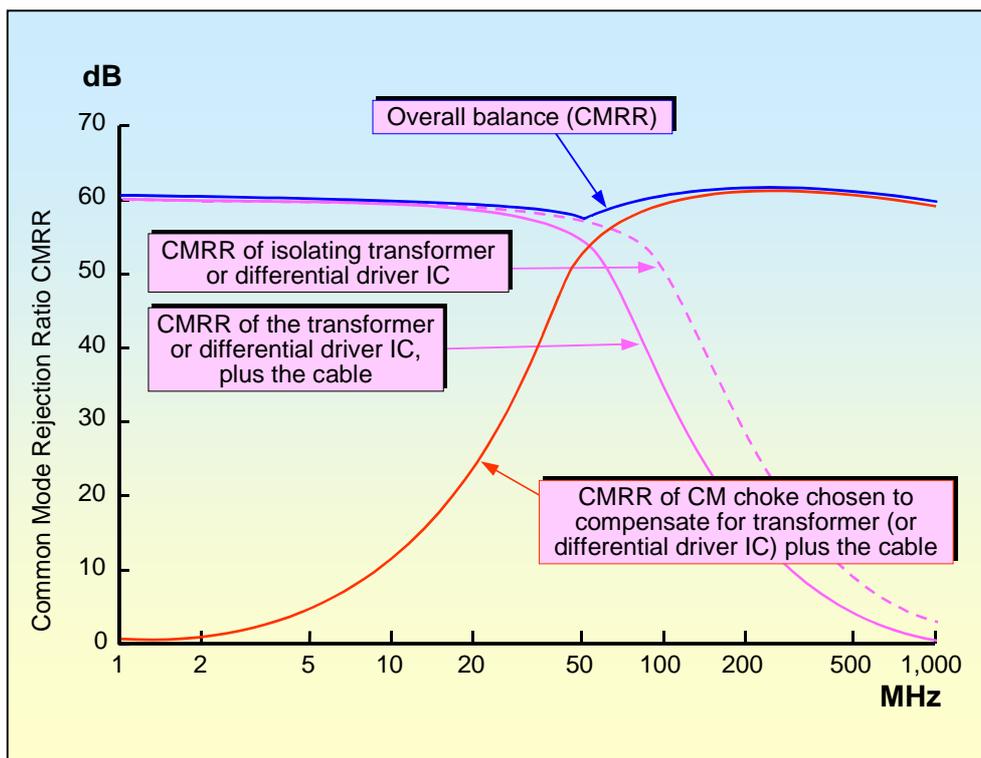


Figure 1R Choose magnetic components to achieve good balance (high CMRR) over the whole frequency range of concern (d.c. to 1GHz in this example)

Where a balanced send or receive IC is used, the 'IC side' winding of the transformer could be centre-tapped instead of the 'cable side', and the centre tap connected to the 0V (via a capacitor if necessary for biasing reasons) to provide CM rejection. Maybe improved performance could be had by centre-tapping both windings and RF bonding them both to their respective references.

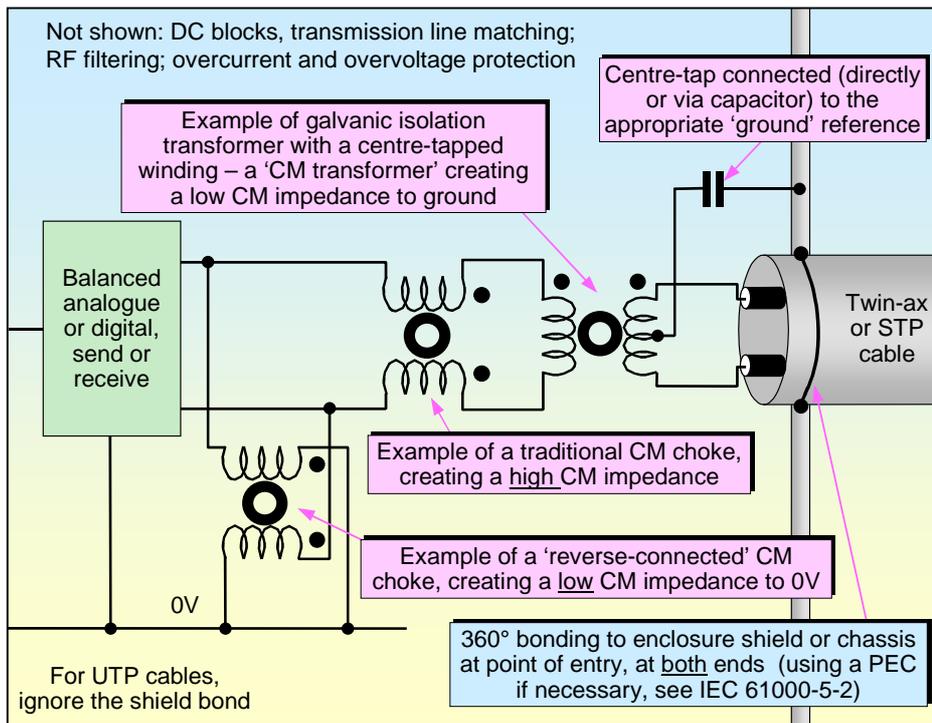


Figure 1S 'CM transformers' and 'reverse-connected' CM chokes

Another alternative to the 'traditional' CM choke is to connect one in reverse [20], as shown in Figure 1S. This creates a low impedance to CM noise, like the CM transformer it closely resembles. The low CM impedance of the CM transformer and reverse-connected CM choke techniques contrasts with the high CM impedance of the more traditional CM choke, so combining these CM suppression techniques in one circuit, as shown in Figure 1S, can provide very powerful CM suppression. Some manufacturers provide magnetic components for serial datacommunications that combine one or more CM chokes, isolation transformers and CM transformers in a small module.

Where co-axial cables are used instead of twisted-pairs or twin-ax, EMC and signal integrity will suffer because the cable isn't a balanced type, and also because the shield carries the signal return current as well as the noise currents due to RF fields, and potential difference between the products at both ends. The techniques shown in Figure 1T will help to achieve the best possible performance from coaxial cables used. Circuits without isolation transformers will generally suffer from poorer immunity at lower frequencies.

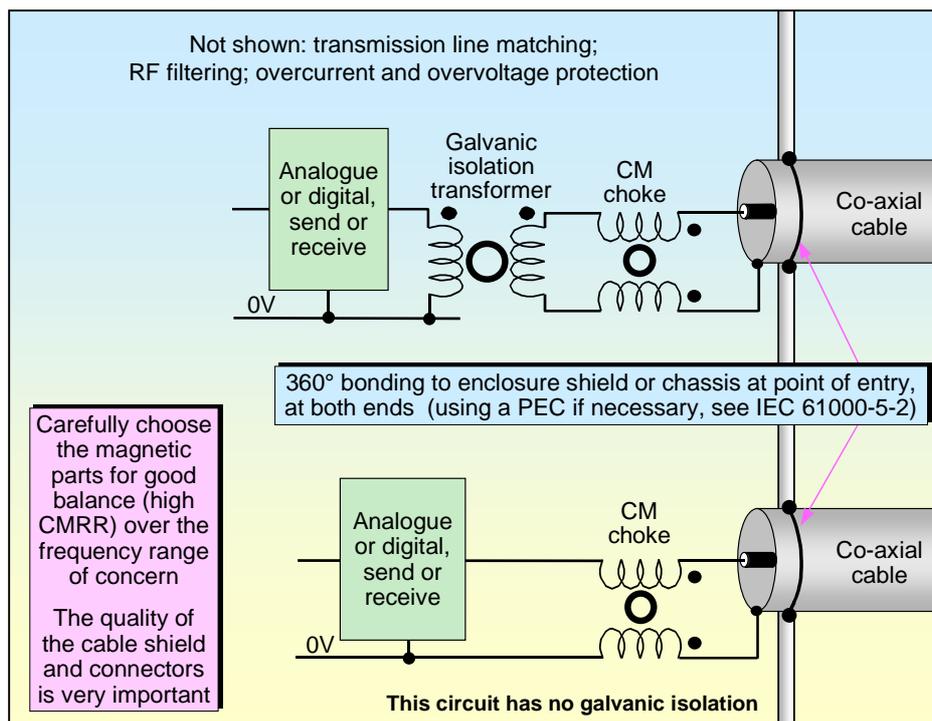


Figure 1T Co-axial cable communications circuits

Low performance datacommunications often use multi-conductor cables to save cost, as shown by Figure 1U, an example of an RS232 application. The EMC of these will generally benefit from the use of CM chokes – where a conductor has N cores, it is generally best to connect it to the electronics at each end via a CM choke with N windings.

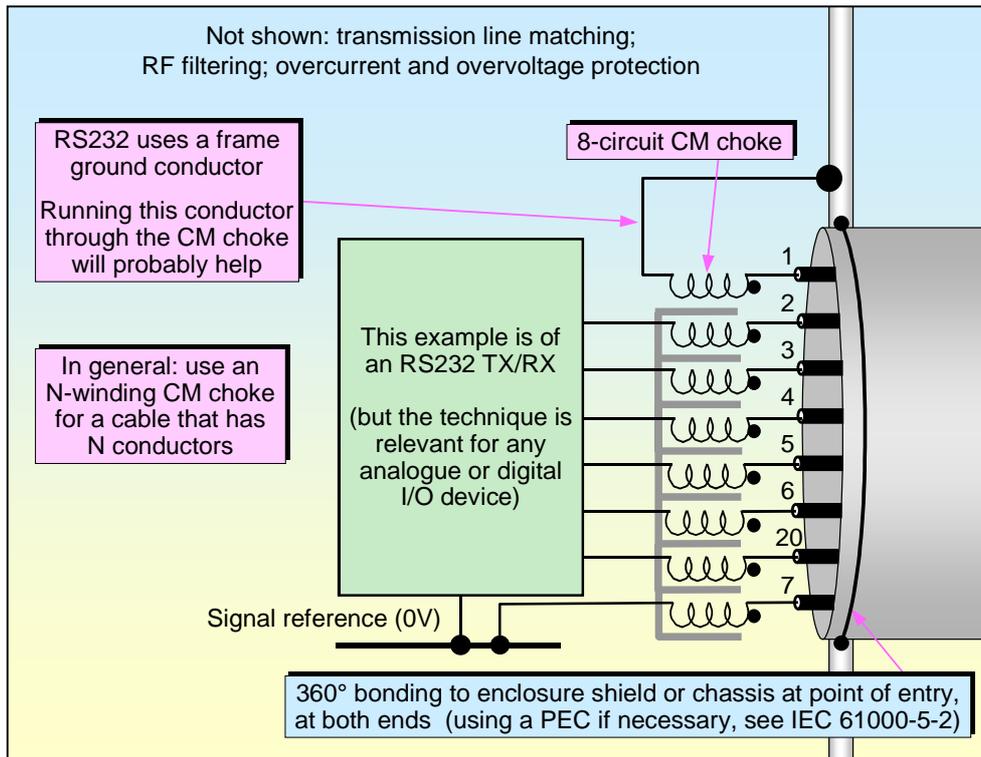


Figure 1U Example of low-rate datacommunications (RS232 in this case)

1.5.3 Opto-coupling and opto-isolation

Opto isolation/coupling techniques using packaged devices are commonly used, especially for digital signals, but the input-output stray capacitance associated with typical devices is a little under 1pF – a high enough value to create a low impedance at frequencies above 100MHz to interact with the circuit impedances and destroy the balance of the signals in the cable, or to interfere with the circuits on the circuit side of the opto device.

Where signals with very short rise/fall times are to be communicated, it may be necessary to employ a suitable CM choke to maintain the balance at high frequencies, as shown by Figure 1V.

But where opto-couplers are used for slow data signals they often use unbalanced coaxial cables, or multi-conductor cables with a single wire for each signal (and a common return). In these cases a single soft ferrite bead in series with each signal line to an opto-coupler may be all that is needed to prevent RF interference.

Opto devices are available with very low input-to-output stray capacitance, achieved by the use of a short light-pipe inside. These are usually intended for high-voltage use. There are also opto devices available with internal shields, usually intended for use in feedback loops in switch-mode power converters and designed to withstand very high levels of noise at frequencies up to 1MHz or so. Although these devices will provide better EMC performance, most of them are not intended for use with very high data rates, very short rise/fall times, or very high frequency analogue signals.

Analogue signals can now benefit from opto-isolation with 0.1% linearity, using devices such as the IL300. This can save having to use voltage-frequency (and frequency-voltage) converters in many opto-coupled applications, or replace bulky transformers.

Because of the common drawing practice of not showing power rails in full on schematics, it sometimes happens that both sides of an opto-isolator are accidentally powered from the same DC power rails, seriously compromising the isolation achieved and the EMC performance. The RF performance of opto-isolators can only be as good as the RF isolation between the power supplies associated with each side of an opto device.

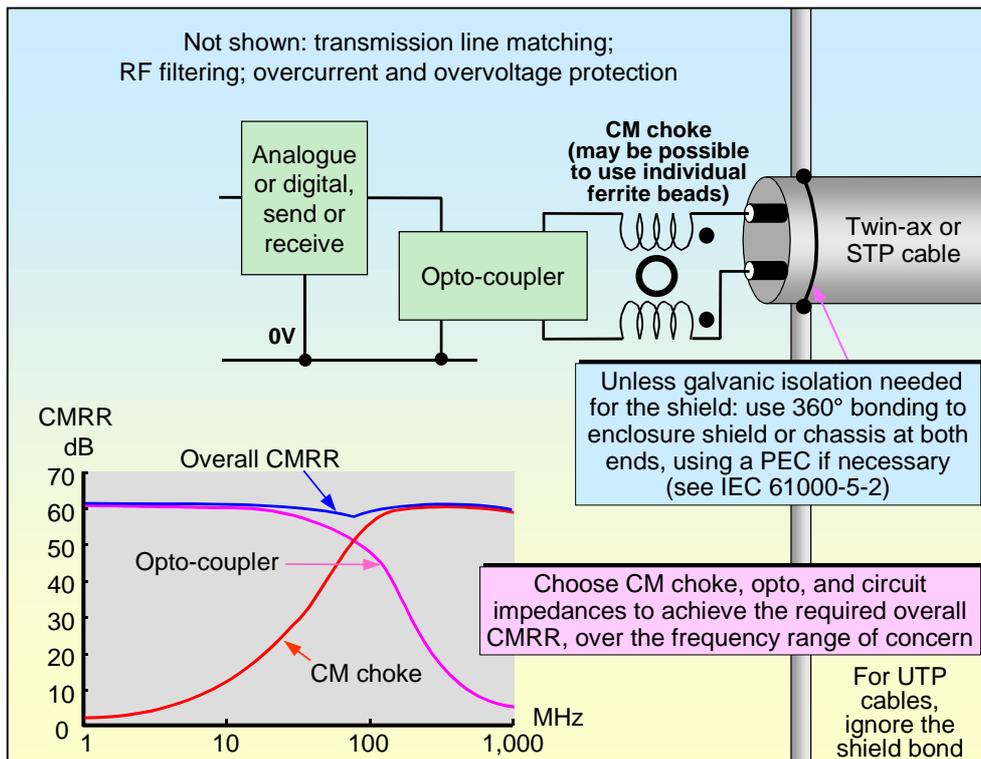


Figure 1V Example of very high-data rate optocoupling

1.6 Quick and easy in-house tests help choose active devices

It is usually the case that a device's real-life EMC performance is unknown, despite the claims made by its suppliers. There are easy and quick EMC testing methods that can be applied in-house, on simple functional circuits that at least run the clocks and preferably perform signal or data I/O operations at full speed too. Some suppliers offer evaluation boards that can be used for these tests.

Testing for emissions can easily be done in a few minutes on a standard test bench with a close-field magnetic loop probe connected to a spectrum analyser or wideband oscilloscope (see Parts 1 and 2 of [7]). Some devices will very quickly be seen to be much quieter than others.

Testing for immunity can use the same probe connected to the output of a signal generator (either continuous RF or transient) – but if it is a proprietary probe (and not just a shorted turn of wire) first check that its power handling is adequate. Refer to Parts 3, 4 and 5 of [7] for appropriate techniques.

Close-field probes need to be held almost touching the devices or PCBs being probed. To locate the “hottest spots” and optimise probe orientation they should first be scanned in a horizontal and vertical matrix over the whole area (holding the probe in different orientations at 90° to each other for each direction), then concentrating on the areas with the strongest signals.

Some digital ICs radiate emissions strongly from their own bodies, rather than conduct them through their pins. They may benefit from being shielded with their own little metal box soldered to the PCB's 0V plane. Shielding at PCB level is very low-cost, and is covered in the forthcoming Parts 4 and 5 of this series, Parts 4 and 5 of [1], and in more detail in Part 2 of [3].

A very few manufacturers offer a few of their IC products with guaranteed EMC emissions and immunity specifications, usually measured in bench-top testers. These are more likely to be complex ICs for use in cellphones and similar products.

1.7 Quick, easy tests on active devices help maintain EMC in serial manufacture

Batches of ICs from the same manufacturers can have different EMC performances, due to the use of silicon processes with smaller features. Device manufacturers are constantly reducing the silicon feature sizes of their devices to fit more of them on a wafer and reduce their costs. This is especially true for digital ICs, where they call it ‘mask-shrinking’ or ‘die-shrinking’.

Larger purchasers can arrange to get advance warnings of mask-shrinks so they can buy enough of the ‘old’ ICs to keep them in production while they find out how to deal with the changed EMC from the new mask-

shrunk IC. Even with 6 months warning, the EMC consequences are known to have cost at least one large manufacturer tens of millions of US dollars.

It is possible to perform simple checks of IC EMC performance when active devices are first delivered to the 'goods-receiving' department, to see whether they have different EMC performance, for whatever reason. This helps discover problems early on, and reduces financial risks. Alternatively, or in addition, sample-based EMC testing in serial manufacture helps avoid shipping non-compliant or unreliable products. Some EMC test methods suitable for use in goods-receiving and manufacturing test are described in [7].

1.8 Choosing passive components

1.8.1 The effects of parasitic R, L and C

All passive components suffer from 'parasitic' resistance, inductance and capacitance (often called stray R, L and C). At a high enough frequency these will dominate the impedance of the components and completely alter their circuit behaviour. Helpful manufacturers of quality components publish data on strays, the most useful being their impedance versus frequency over the range of frequencies of concern. (Never choose a ferrite suppressor without such a curve.)

For example, at high frequencies a leaded film resistor can act either as a capacitor (due to its shunt C of around 0.2pF) or as an inductor (due to the L of its leads plus its spiralled tolerancing cut). Wire-wound resistors above a few kHz have an impedance which is not what was marked on their box (even 'low-inductance' types), whereas leaded film resistors under 1kΩ usually remain resistive up to a few hundred MHz. See Figure 1W for a simplified analysis of typical surface mounted resistors.

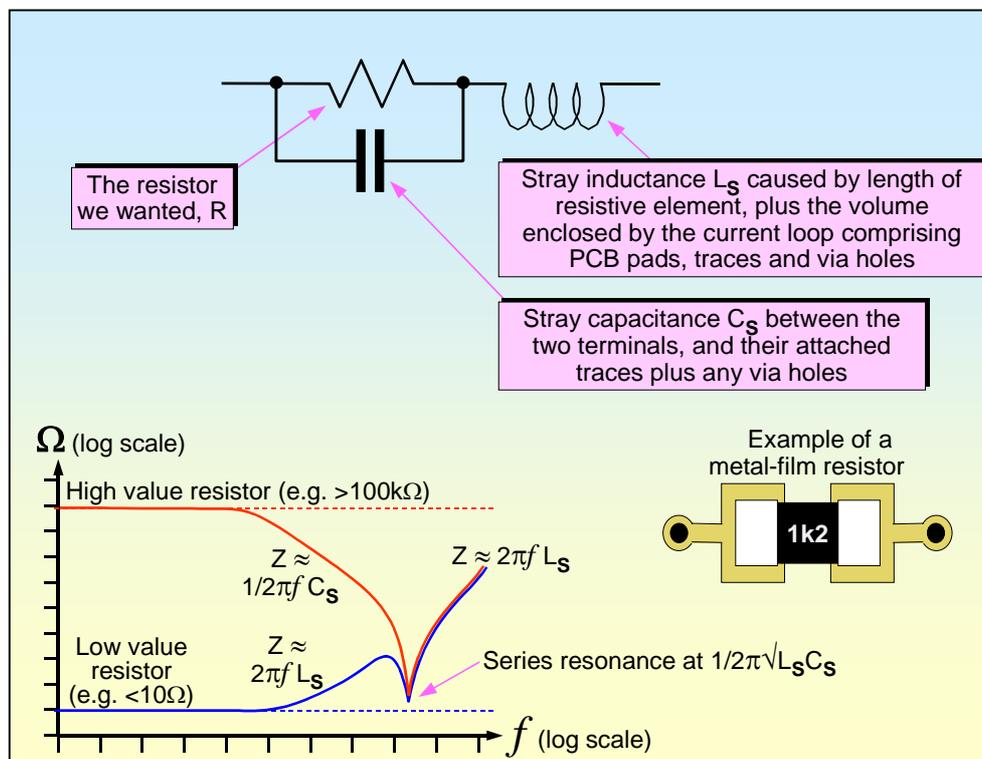


Figure 1W Example of a first-order equivalent circuit for a surface mounted resistor

Capacitors self-resonate due to their internal interconnect inductance, and at higher frequencies their impedances are mostly inductive, see Figure 1X for a simplified analysis of a typical multilayer ceramic surface mounted capacitor.

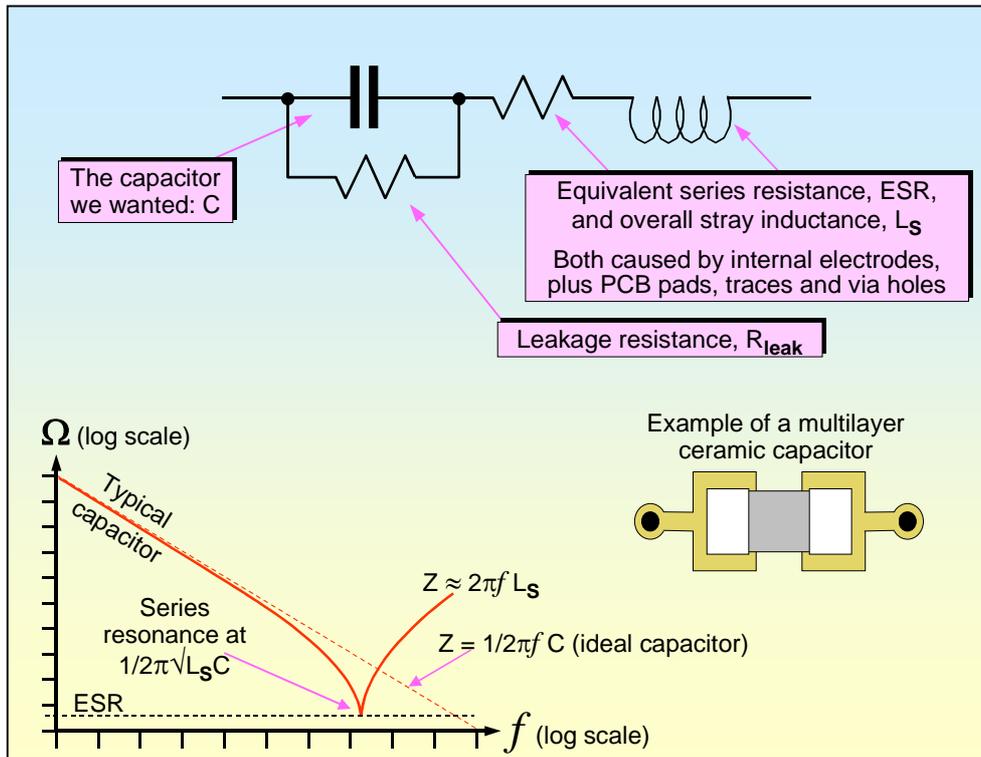


Figure 1X Example of a first-order equivalent circuit for a surface mounted capacitor

Inductors self-resonate due to their internal and interconnect inductance, and their interwinding capacitance. See Figure 1Y for a simplified analysis of a typical surface mounted inductor (note: this is *not* a soft-ferrite RF suppressor type).

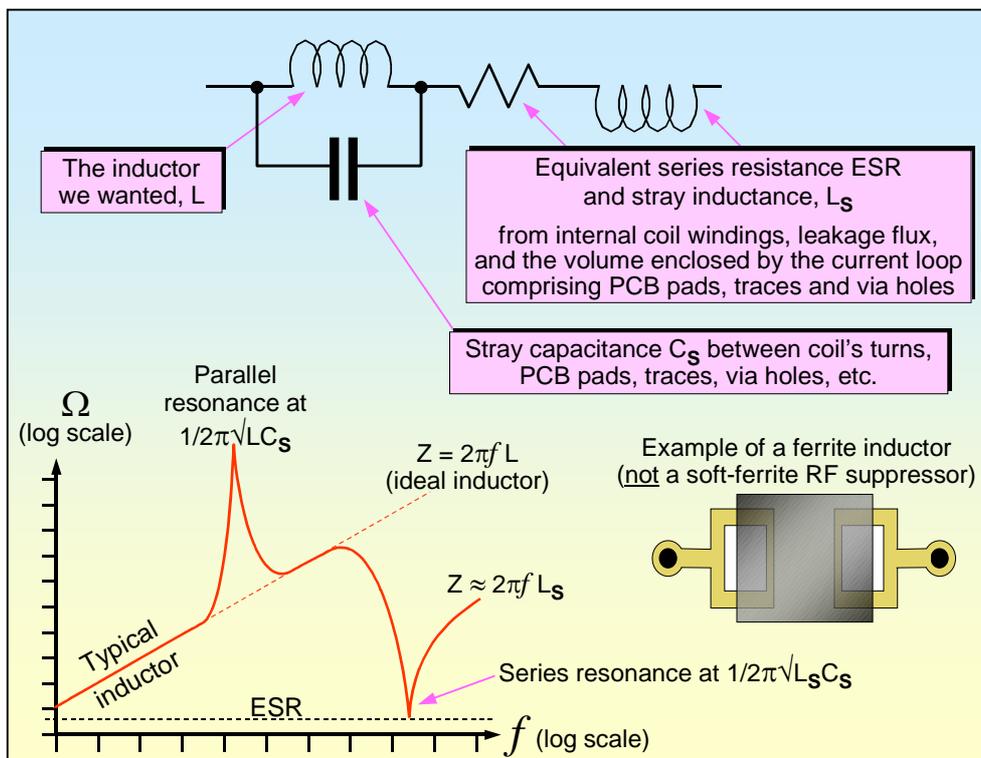


Figure 1Y Example of a first-order equivalent circuit for a surface mounted inductor

Where leaded components are important for good EMC, their lead lengths should be well-controlled in serial manufacture (just adding 5mm of lead length to a PCB-mounted component can completely ruin its RF and EMC characteristics). Surface mounted components are preferred for EMC because they cannot suffer from lead-length variations, plus they are smaller so their strays are generally lower, so they generally maintain their nominal values up to a much higher frequency. For example, SMD 'chip' resistors under 1kΩ (but not MELF types) are usually resistive to at least 1GHz.

All components have a limited power handling capacity (both transient and continuous dissipation ratings), a limited dV/dt capacity (e.g. tantalums go short-circuit if their dV/dt limit is exceeded), a limited dI/dt capability, etc. SMD parts, being smaller, generally have lower wattage ratings than leaded parts.

The parasitic Rs, Ls and Cs in passive components makes filter design much more complicated than the circuits in textbooks or on computer simulators might suggest. Where a passive component is to be used with high frequencies (e.g. to divert interfering currents up to 1GHz to a 0V plane) it is vital to understand all about its strays and to do a few simple sums to work out their effects.

The use of components with unknown parasitics for high-speed signals and/or EMC purposes makes it more likely that the number of product design iterations will be high and time-to-market delayed.

1.8.2 Choosing capacitors

Ceramic dielectrics usually give the best high frequency performance, so SMD ceramics are often excellent. Some ceramic dielectrics have strong temperature or voltage coefficients, but COG or NPO dielectric materials have no significant temperature, frequency, or voltage coefficients, so make very stable and rugged high-quality high-frequency or pulse-handling capacitors.

There are many other issues relating to selection of capacitors, including RF impedance, pulse-handling capability, equivalent series resistance (ESR), equivalent series inductance (ESL), tolerance, ageing, etc. Very low ESR is a very important EMC requirement for the bulk storage capacitors in switch-mode power converters.

Electrolytic capacitors are ineffectual at frequencies above a few MHz, so often need to be paralleled with ceramic capacitors. Replacing electrolytics completely with multilayer ceramic capacitors (MLCC) is often a good thing for EMC and long-term reliability – it seems that the lower ESRs of the MLCCs (now available with up to 100 μ F in small case sizes at low DC voltage) means that an electrolytic can be replaced by an MLCC that has between one-half and one-fifth of its value, depending on the application.

1.8.3 Choosing or designing magnetic components

The magnetic circuits of inductors and transformers should be closed to reduce magnetic field emissions, for example by using toroids or other types of gapless cores, for immunity as well as for emissions. Rod-cored chokes or inductors must be used with great care, if they cannot be avoided altogether. Inductors wound on ferrite rods make good RF antennas (and are used for that purpose in AM radios) – not what we need for good EMC. Toroidal mains transformers in linear power supplies are gapless, and can have lower 'hum' fields than standard rectangular core types.

Energy storage inductors in switch-mode converters must have an air gap, but iron powder toroidal types effectively store their energy in the microscopic air gaps between the iron particles, distributed around the body of the toroid, so emit lower fields than gapped cores.

If air gaps *have* to be used, an overall shorted turn may be needed to reduce the leakage fields. It is important to understand that 'overall' means that the turn is around the entire body of the component, so that it is only a shorted turn for the leakage fields. Shorting turns are used to reduce emissions from switch-mode power converter magnetics, and also to improve the immunity of microphone and other sensitive transformers.

The current flowing in an inductor directly affects its inductance value, so it is important to know what this coefficient is to design circuits (e.g. filters) correctly. High temperatures also have an effect on inductance, as temperatures rise above about 50°C inductance falls more and more quickly until the Curie point is reached, at which temperature the material loses all its inductance (cooling below the Curie point restores the inductance).

Other issues to consider in the choice of magnetic components include saturation (when inductance drops to zero) and the possibility of overheating due to dissipation in both core and the windings. Ferrite cores are not insulators, so in some cases may need to be coated with a tough insulator.

1.8.4 Safety issues

Some active devices and passive components will need to be rated for safety, especially all those connected to hazardous voltages such as the AC mains supply. In such cases it is best to only use parts which have been approved to the correct safety standard(s) at the correct ratings by an accredited third-party laboratory and allowed to carry their distinguishing mark (e.g. VDE, UL, CSA, SEMKO, DEMKO, NEMCO, BSI, TUV, etc. But you can't rely on the presence of an agency mark on the component, or on its data sheet – they could be forgeries.

Due diligence in safety requires getting a copy of the safety approval certificates and/or test reports for the components concerned, and then...

- checking with the issuing laboratories that they are not forgeries,
- checking that their tested ratings are what you need for your design,

- checking that they fully comply with all the parts of all the necessary safety standards for your design.

A procedure should also be in place to check that components delivered for assembly into a manufacturer's products are not counterfeit. About 5% of world trade is estimated to be counterfeit, including such safety-related components such as mains cords, fuses and circuit-breakers. This is public knowledge, so if a counterfeit component caused a safety incident the manufacturer might be held fully liable under the Low Voltage Directive, General Product Safety Directive, or Product Liability Directive for not taking the necessary precautions.

1.9 Second-sourced components

ICs, transistors and passive components from different manufacturers can have very different EMC performances even if they have the same part number and data sheet specifications. Costly test laboratory EMC testing on products fitted with second-source components may not be required on the second-source devices, however, where appropriate quick and easy in-house tests (see [7]) show no significant differences for emissions or immunity. If no EMC testing is to be done on the second-sourced components it will be best to use single sourced devices.

1.10 Some mechanical design and assembly issues

- *Place noisy or sensitive devices as far from conductors as possible.* Noisy devices include all crystal oscillators, ICs and transistors that operate at high clock speeds. Conductors include PCB traces, connectors, wires, cables, structural elements (e.g. brackets), etc. When a product is finally assembled, flexible wires, cables and other conductors inside its enclosure can often lie in a wide variety of positions – it is very important to ensure that no such wires or cables might lie on top of (or nearby) any high-speed digital or data conversion, or sensitive analogue devices.
- *'Ground' heatsinks.* A heatsink is a conductor, and clearly must have at least a part of itself in intimate proximity to the device it is cooling. But heatsinks can suffer from coupled signals from inside an IC just like any other conductor. The usual technique is to isolate the heatsink from the IC with a thermal conductor (the thicker the better as long as thermal dissipation targets are met), then 'ground' the heatsink to the PCBs 0V plane local to the device being cooled with many very short connections (the mechanical fixings can often be used). To reduce radiation at 100MHz and above, a heatsink needs evenly distributed 0V connections all around its perimeter – better still, a continuous peripheral connection via a conductive gasket. See Part 8 of [3] for more on this.
Heatsinks for off-line switchers were discussed earlier – be sure to deal fully with all possible safety issues.
- *Avoid sockets.* IC sockets are very bad for EMC, and directly soldered surface-mounted ICs (or chip and wire, or similar direct chip termination techniques) are preferred. Where motherboards are fitted with ZIF sockets and spring-mounted heatsinks to allow easy processor upgrading, EMC performance will not be the best and the additional filtering and shielding performance required will increase costs. It will help to choose surface-mounted ZIF sockets with the shortest lengths of internal metalwork for their contacts.
- *Use smaller, lower profile IC packages.* These can give improved emissions and immunity on PCBs fitted with 0V planes (see the forthcoming Part 5 of this series, Part 5 of [1], or Part 4 of [3]). Very small devices (e.g. chip-scale packaging, flip chip, micro-BGA) can be used to produce very low-cost PCBs with very good EMC if advanced PCB design and manufacturing techniques [3] are used.

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